Reconfigurable Architectures Workshop (RAW) 2015
Keynote Talk

FPGAs for Telecom and Graph Analytics

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As the Information and Communication (ICT) infrastructure continues to evolve, throughput and energy efficiency have become key metrics. This talk explores FPGA-based parallel architectures and algorithms for a variety of streaming applications arising in Telecom and Big Data. We show high performance accelerators for deep packet inspection, regular expression matching, packet classification, traffic classification, heavy hitter detection, etc. in core routers, data center networks and in software defined networking (SDN). We propose high throughput and energy efficient accelerator designs to realize the "Green ICT" vision. Our approach is based on high level abstractions of the reconfigurable platforms and efficient data structures and algorithms. We illustrate the performance improvements for such systems and demonstrate the suitability of FPGAs for these computations. We show that SRAM/DRAM based solutions combined with FPGA based architectures lead to high throughput as well as reduced power dissipation compared with the state-of-the-art solutions based TCAMs. We then consider hardware support for Big Data applications. We show high throughput and energy optimal solutions for sorting, data base and graph analysis. We introduce the notion of energy balanced architectures to understand tradeoffs between power and performance in application specific architectures and show algorithmic optimizations to effectively use the hardware resources of FPGAs. We also show comparisons with multi-core and GPU implementations.

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