# Reconfigurable Architectures Workshop (RAW) 2015

May 25, 2015, Hyderabad, India

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| 8:00-8:15 am | Registration | |
| 8:15-8:30 am | Opening Remarks | |
| 8:30-9:30 am | **Keynote: FPGAs for Telecom and Graph Analytics**<br>Viktor K. Prasanna, University of Southern California | |
| 9:30-10:00 am | Coffee Break | |
| 10:00-11:40 am | **Session 1: Runtime and Tools for Partially Reconfigurable FPGA-Based Systems**<br>Chair: TBA | |
| | Mini-NOVA: A Lightweight ARM-based Virtualization Microkernel Supporting Dynamic Partial Reconfiguration | T. Xia, J. C. Prévotet and F. Nouvel |
| | Real-Time Multiprocessor Architecture for Sharing Stream Processing Accelerators | B. Dekens; M. Bekooij and G. Smit |
| | Partial Region and Bitstream Cost Models for Hardware Multitasking on Partially Reconfigurable FPGAs | A. Morales-Villanueva and A. Gordon-Ross |
| | Relocation-Aware Floorplanning for Partially-Reconfigurable FPGA-based Systems | M. Rabozzi, R. Cattaneo, T. Becker, W. Luk and M. Santambrogio |
| 11:40 am-12:10 pm | Interactive Session | |
| 12:10-1:10 pm | Lunch | |
| 1:10-1:35 pm | Short Paper Introduction Session<br>Chair: TBA | |
| | An Automated High-level Design Framework for Partially Reconfigurable FPGAs | R. Kumar and A. Gordon-Ross |
| | Intermediate-Level Synthesis of a Gauss-Jordan Elimination Linear Solver | M. A. Daigneault and J. P. David |
| | K-Ways Partitioning of Polyhedral Process Networks: a Multi-Level Approach | R. Cattaneo, M. Moradmand, D. Sciuto and M. Santambrogio |
| | Estimation of Non-Functional Properties for Embedded Hardware with Application to Image Processing | C. Herglotz, J. Seiler, A. Kaup, A. Hendricks, M. Reichenbach and D. Fey |
| | Adaptive Reconfigurable Architecture for Image Denoising | K. Hegde, V. Kulkarni, R. Harshvardhan and S. David |
| 1:35-3:15 pm | Session 2: Applications and Special Purpose Architectures with Reconfigurable Hardware<br>Chair: TBA | |
| | High-Throughput Online Hash Table on FPGA | D. Tong, S. Zhou and V. K. Prasanna |
| | GraphMMU: Memory Management Unit for Sparse Graph Accelerators | N. Kapre, J. Han, P. Moorthy and Siddhartha |
| | Adaptive Recursive Doubling Algorithm for Collective Communication | O. Arap, M. Swany, G. Brown and B. Himebaugh |
| | Accelerating Large-Scale Single-Source Shortest Path on FPGA | S. Zhou, C. Chelmis and V. K. Prasanna |
| 3:15-4:00 pm | Interactive Session and coffee break | |
| 4:00-5:40 pm | Session 3: New Architectures and Performance Evaluation for Reconfigurable Computing<br>Chair: TBA | |
| | Experiences with Compiler Support for Processors with Exposed Pipelines | N. Jensen, P. Schleuniger, A. Hindborg, M. Walter and S. Karlsson |
| | An Architecture for Configuring an Efficient Scan Path for a Subset of Elements | A. Ashrafi and R. Vaidyanathan |
| | Performance Modeling of Matrix Multiplication on 3D Memory Integrated FPGA | S. Singapura, A. Panangadan and V. K. Prasanna |
| | Enhancing Speedups for FPGA Accelerated SPICE through Frequency Scaling and Precision Reduction | N. Kapre and L. H. Hui |
| 5:40-6:10 pm | Interactive Session | |
| 6:10-6:30 pm | Closing Remarks | |