RAW 2014 Advance Program

Monday, May 19, 2014

8:00-8:15	Registration	
8:15-:8:30	Opening Remarks	
8:30-:9:30	RAW Keynote 1	
	Joshua Walstrom, Altera Corporation, USA.	Runtime Reconfiguration in Altera FPGAs - Past, Present, and Future
9:30-10:00 am	Coffee break	
10:00-11:15 am	**Session 1: Compilers and Binary Translation for Reconfigurable Architectures**	
	Doug Gallatin, Aaron Keen, Chris Lupo and John Oliver	Twill: A hybrid Microcontroller-FPGA Framework for Parallelizing Single-Threaded C Programs
	Ali Mustafa Zaidi and David Greaves	A New Dataflow Compiler IR for Accelerating Control-Intensive Code in Spatial Hardware
	Toan Mai and Jongeun Lee	Efficient Software-based Runtime Binary Translation for Coarse-Grained Reconfigurable Architectures
11:15-11:40 am	**Day 1 Poster Introductions**	
11:40-12:05 pm	**Interactive Session 1**	
12:05-1:30 pm	Lunch (on your own)	
1:30-2:45 pm	**Session 2: New Reconfigurable Architectures**	
	Georgios Smaragdos, Danish Anis Khan, Ioannis Sourdis, Christos Strydis, Alirad Malek and Stavros Tzilis	A Dependable Coarse-grain Reconfigurable Multicore Array
	Cuong Pham-Quoc, Zaid Al-Ars and Koen Bertels	Automated Hybrid Interconnect Design for FPGA Accelerators Using Data Communication Profiling
	Anil Kumar Sistla, Xiaozhong Luo, Mukund Malladi, Marc Reisner, Rajasekhar Ganduri and Gayatri Mehta	SmartBricks: A visual environment to design and explore novel custom domain-specific architectures
2:45-3:10 pm	**Interactive Session 2**	
3:10-3:40 pm	Coffee break	
3:40-4:55 pm	**Session 3: ViPES Session**	
	Harry Sidiropoulos, Kostas Siozios and Dimitrios Soudris	Framework for Mapping Dynamic Virtual Kernels onto Heterogeneous Reconfigurable Platforms
	Andreas Emeretlis, George Theodoridis, Panayiotis Alefragis and Nikolaos Voros	A hybrid ILP-CP model for mapping Directed Acyclic Task Graphs to multicore architectures
	Kostas Siozios, Dimitrios Soudris and Michael Huebner	A Framework for Customizing Virtual 3-D Reconfigurable Platforms at Run-Time
4:55-5:20	**Interactive Session 3**	
5:20-6:30pm	**Panel Discussion**	

Day 1 Posters	
Hiroki Nishiyama, Masato Inagi, Shin'Ichi Wakabayashi, Shinobu Nagayama, Keisuke Inoue and Mineo Kaneko	An ILP-based Optimal Circuit Mapping Method for PLDs
Cristiano Bacelar De Oliveira, Joao Cardoso and Eduardo Marques	High-Level Synthesis from C vs. a DSL-based Approach
Zhang Zhang, Swamy Ponpandi and Akhilesh Tyagi	An Evaluation of User Satisfaction Driven Scheduling in a Polymorphic Embedded System
Georgios Tzimpragos, Christoforos Kachris, Dimitrios Soudris and Ioannis Tomkos	A Low-Latency Algorithm and FPGA Design for the Min-Search of LDPC Decoders
Jahanzeb Anwer, Marco Platzner and Sebastian Meisner	FPGA Redundancy Configurations: An Automated Design Space Exploration

Tuesday, May 20, 2014

8:30-9:30 am	IPDPS Keynote	
9:30-10:00 am	Coffee Break	
10:00-11:00 am	RAW Keynote 2	
	Maya Gokhale, Lawrence Livermore National Lab., USA	Reconfigurable Architectures for Extreme Scale Computing
11:00-12:15	**Session 4: Circuit-level Applications**	
	Rui Policarpo Duarte and Christos-Savvas Bouganis	Over-Clocking of Linear Projection Designs Through Device Specific Optimisations
	Michael Raitza, Markus Vogt, Christian Hochberger and Thilo Pionteck	Influence of Magnetic Fields and X-Radiation on Ring Oscillators in FPGAs
	Takumi Fujimori and Minoru Watanabe	Radiation tolerance of color configuration on an optically reconfigurable gate array
12:15-1:30 pm	Lunch (on your own)	
1:30-1:55 pm	**Day 2 Poster Introductions**	
1:55-2:20 pm	**Interactive Session 4**	
2:20-3:10 pm	**Session 5: Numerical Reconfigurable Computing Applications**	
	Esti Stein and Yosi Ben-Asher	Adaptive Booth Algorithm for Three-integers Multiplication for Reconfigurable Mesh
	Xinying Wang and Joseph Zambreno	An FPGA Implementation of the Hestenes-Jacobi Algorithm for Singular Value Decomposition
3:10-3:35 pm	**Interactive Session 5**	
3:35-4:05 pm	Coffee break	
4:05-5:20 pm	**Session 6: Applications of Reconfigurable Computing**	
	Osama Attia, Tyler Johnson, Kevin Townsend, Philip Jones and Joseph Zambreno	CyGraph: A Reconfigurable Architecture for Parallel Breadth-First Search
	Gianluca Durelli, Fabrizio Spada, Riccardo Cattaneo, Christian Pilato, Danilo Pau and Marco Domenico Santambrogio	Adaptive Raytracing Implementation using Partial Dynamic Reconfiguration
	Riccardo Cattaneo, Riccardo Bellini, Gianluca Durelli, Christian Pilato, Marco Domenico Santambrogio and Donatella Sciuto	PaRA-Sched: a Reconfiguration-Aware Scheduler for Reconfigurable Architectures
5:20-5:45 pm	**Interactive Session 6**	
5:45-6:00 pm	Closing remarks	

Day 2 Posters	
Chen Mei, Peng Cao, Yang Zhang, Bo Liu and Leibo Liu	Hierarchical Pipeline Optimization of Coarse Grained Reconfigurable Processor for Multimedia Applications
Alexander Wold, Andreas Agne and Jim Torresen	Module Placement using Constraint Programming in Run-time Reconfigurable Systems
Hasan Erdem Yantir and Arda Yurdakul	An Efficient Heterogeneous Register File Implementation for FPGAs
Bernhard Schmidt, Daniel Ziener and Jürgen Teich	Minimizing Scrubbing Effort through Automatic Netlist Partitioning and Floorplanning
Duy Viet Vu, Timo Sandmann, Steffen Baehr, Oliver Sander and Juergen Becker	Virtualization Support for FPGA-based Coprocessors Connected via PCI Express to an Intel Multicore Platform