RAW 2013 Advance Program

Monday, May 20, 2013

8:00-8:15 Registration

8:15-:8:30 Opening Remarks

8:30-:9:30 RAW Keynote 1

Jaime Cummins, CEO, Pico Computing	Unleashing Software Developers into the World of Reconfigurable Computing/Logic

9:30-10:30 am Coffee break

10:30-11:45 am **Session 1: Systems and Applications (Chair: René Cumplido)**

Lingkan Gong, Oliver Diessel, Johny Paul and Walter	RTL Simulation of High Performance Dynamic
Yun Qu and Viktor Prasanna	High-performance Pipelined Architecture for Tree-based IP lookup Engine on FPGA
Andrea Sanny, Thilan Ganegedara and Viktor Prasanna	A Comparison of Ruleset Feature Independent Packet Classification Engines on FPGA

11:45-12:10 pm **Day 1 Posters Introduction (Michael Hübner)**

12:10-1:45 pm Posters Lunch (on your own)

1:45-3:00 pm **Session 2: Architectures and Algorithms I (Chair: Marco D. Santambrogio)**

Bjoern Liebig, Jens Huthmann and Andreas Koch	Architecture Exploration of High-Performance Floating-Point Fused Multiply-Add Units and their Automatic Use in High Level Synthesis
Jingfei Jiang, Rongdong Hu and Mikel Lujan	A Flexible Memory Controller Supporting Deep Belief Networks with Fixed-Point Arithmetic
Jan Heisswolf, Andreas Weichslgartner, Muhammad Aurang Zaib, Ralf König, Thomas Wild, Andreas Herkersdorf, Juergen Teich and Juergen Becker	Hardware Supported Adaptive Data Collection for Networks on Chip

3:00-3:45 pm Coffee break and posters

3:45-5:00 pm **Session 3: Software and Tools I (Chair: Eduardo de la Torre)**

Wenwei Zha and Peter Athanas	An FPGA Router for Alternative Reconfiguration
Kizheppatt Vipin and Suhaib A. Fahmy	An Automated Partitioning Scheme for Partial Reconfiguration based Adaptive Systems
Ángel Gallego, Javier Mora, Andrés Otero, Rubén Salvador, Eduardo De La Torre and Teresa Riesgo	A Novel FPGA-based Evolvable Hardware System based on Multiple Processing Arrays

5:00-5:15 pm break

5:15-6:15pm **Panel Discussion: The Next 20 Years of Reconfigurable Computing**

Day 1 Posters

Indranil Hatai, Swapna Banerjee and Indrajit Chakrabarti	Reconfigurable Architecture of a RRC FIR Interpolator for Multi-Standard Digital Up Converter
Pierre Bomel, Kevin Martin and Jean-Philippe Diguet	Standard-IOs based on Dynamically Allocated Virtual UARTs for Reconfigurable Multi-Processor Architectures on Hybrid FPGAs (Zynq case study)
George Afonso, Rabie Benatitallah, David Duvivier, Zeineb Baklouti and Geoffroy Pertuisot	Heterogeneous CPU/FPGA Reconfigurable Computing System for Avionic Test Application
Michael Mefenza and Christophe Bobda	FPGA Implementation of Subcarrier Index Modulation OFDM Transceiver
Roland Christian Gamom Ngounou Ewo, Emmanuel Kiegaing, Martin Mbouenda, Hilaire Bertrand Fotsin and Bertrand Granado	Hardware MPI-2 functions for Multi-Processing Reconfigurable System on Chip

Tuesday, May 21, 2013

8:30-9:30 am IPDPS Keynote

9:30-10:30 am Coffee Break

RAW Keynote 2

10:20-11:30 am	Ivo Bolsens, Senior Vice President and CTO, Xilinx	The All Programmable SOC FPGA at the heart of embedded systems

11:45-12:15 **Day 2 Posters Introduction (Diana Göhringer)**

12:15-1:45 pm Posters Lunch (on your own)

Session 4: Architectures and Algorithms II (Chair: Suhaib Fahmy)

Gianluca Durelli, Alessandro A. Nacci, Riccardo Cattaneo, Christian Pilato, Donatella Sciuto and Marco Domenico Santambrogio	A Flexible and Reconfigurable Interconnection Structure for FPGA Dataflow Applications
Kolin Paul, M Balakrishnan and Mansureh Shahraki Moghaddam	Design and Implementation of High Performance Architectures with Partially Reconfigurable CGRAs
Jochem H. Rutgers, Marco J.G. Bekooij and Gerard J.M. Smit	Portable Memory Consistency for Software Managed Distributed Memory in Many-Core SoC

3:00-3:45 pm Coffee break and posters

3:45-5:00 pm **Session 5: Software and Tools II (Chair: Christian Pilato)**

Anilkumar Sistla, Natalie Parde, Krunalkumar Patel and Gayatri Mehta	Cross-Architectural Study of Custom Reconfigurable Devices using Crowdsourcing
Davide Basilio Bartolini, Matteo Carminati, Fabio Cancare, Marco Domenico Santambrogio and Donatella Sciuto	HERA Project's Holistic Evolutionary Framework
Yoon Kah Leow and Ali Akoglu	A Hybrid FPGA Model to Estimate On-Chip Crossbar Logic Utilizations In SoC Platforms

5:00-5:30 pm Closing remarks

Day 2 Posters

Alexander Wold	Thermal Aware Module Placement for Heterogeneous 3D-IC Based FPGAs
Peng Li, Angshuman Parashar, Michael Pellauer, Tao Wang and Joel Emer	A Hierarchical Architectural Framework for Reconfigurable Logic Computing
Pranav Tendulkar and Sander Stuijk	A Case Study into Predictable and Composable MPSoC Reconfiguration
Miho Ueno, Masanori Hashimoto and Takao Onoye	Real-time Supply Voltage Sensor for Detecting/Debugging Electrical Timing Failures
Sergio Cruz, Daniel Muñoz, Carlos Llanos, Geovany Borges and Milton Conde	A Hardware Approach for Solving the Robot Localization Problem using a Sequential EKF