RAW 2012 Program

Monday, May 21, 2012

8:00-8:30	Registration
8:30-8:45	RAW Opening - Chair's Welcome
8:45-10:00	**RAW Keynote 1:** Gordon Brebner, Xilinx Inc., USA. "Domain-Specific Programming of Very High Speed Packet Processing"
10:00-10:20	Short Break
10:20-11:35	**Session 1 - Physical Design of Partially Reconfigurable Architectures**
10:20-10:45	Designing Nonvolatile Reconfigurable Switch-based FPGA Through Overall Circuit Performance Evaluation. KazutakaIkegami, Keiko Abe, Kumiko Nomura, ShinichiYasuda, Masato Oda, ShinobuFujita.
10:45-11:10	A Power and Cluster-Aware Technology Mapping and Clustering Scheme for Dual-VT FPGAs. Wei Ting Loke, Yajun Ha, Wenfeng Zhao.
11:10-11:35	A Comparison of DAG and Mesh Topologies for Coarse-Grain Reconfigurable Array. Jonathan Antusiak, Antoine Trouvé, Kazuaki Murakami.
11:35-12:00	**Introduction to posters 1-5**
12:00-13:15	Lunch
13:15-14:30	**Session 2 - Network on Chip for Reconfigurable Hardware**
13:15-13:40	Hardware-assisted Decentralized Resource Management for Networks on Chip with QoS. Jan Heisswolf, AurangZaib, Andreas Weichslgartner, Ralf König, Thomas Wild, Jürgen Teich, Andreas Herkersdorf, Jürgen Becker.
13:40-14:05	Self-Correction Trace Model: A Full-System Simulator for Optical Network-on-Chip. Mingzhe Zhang, Liqiang He, Dongrui Fan.
14:05-14:30	Real-Time Monitoring of Multicore SoCs Through Specialized Hardware Agents on NoC Network Interfaces. George Kornaros.
14:30-15:00	**Introduction to posters 6-10**

15:00-16:00	**Session 3 - Poster Session (Posters 1-10) & Coffee break**

16:00-18:05	**Session 4 - Improving Security and Computing Efficiency of Reconfigurable Systems**
16:00-16:25	Managing Dynamic Reconfiguration for Fault-tolerance on a Manycore Architecture. Zain Ul-Abdin, Essayas Gebrewahid, Bertil Svensson.
16:25-16:50	Using Run-Time Reconfiguration to Implement Fault-Tolerant Coarse Grained Reconfigurable Architectures. Thomas Schweizer, Anja Kuester, Sven Eisenhardt, Tommy Kuhn, Wolfgang Rosenstiel.
16:50-17:15	On Supporting Efficient Partial Reconfiguration with Just-In-Time Compilation. Harry Sidiropoulos, Kostas Siozios, Peter Figuli, Dimitrios Soudris, Michael Huebner.
17:15-17:40	An Enhanced Relocation Manager to Speedup Core Allocation in FPGA-based Reconfigurable Systems. Marco Domenico Santambrogio, Fabio Cancare, Riccardo Cattaneo, Sheetal Bhandari, Donatella Sciuto.
17:40-18:05	Classification of Massively Parallel Computer Architectures. Muhammad Ali Shami, Ahmed Hemani.

Session 3 Posters

1: High speed -- low power optical configuration on an ORGA with a phase-modulation type holographic memory. Takahiro Watanabe, Minoru Watanabe.
2: Efficient Reconfiguration Algorithm for Three-dimensional VLSI Arrays. Guiyuan Jiang, Jigang Wu, Jizhou Sun.
3: Reconfigurable Processor Arrays with Faults. Jigang Wu, Guiyuan Jiang, Yuanrui Zhang, Yuanbo Zhu.
4: A Heterogeneous Cache Distribution with Reconfigurable Interconnect. Aishwariya Pattabiraman, Annie Avakian, Ranga Vemuri.
5: Study of an Automated Precise SEU Fault Injection Technique. Jing Zhou, Zengrong Liu, Lei Chen.
6: Detecting Data Hazards in Multi-Processor System-on-Chips on FPGA. Chao Wang, Li Xi, Xuehai Zhou, Peng Chen.
7: Mapping Algorithm for Coarse-Grained Reconfigurable Multimedia Architectures. Naijin Chen, Jianhui Jiang.

8: Reconfigurable Designs for Networking Silicon. Tao Li, Zhentao Liu, Huimin Du, Lei Zhang, Jungang Han, Lin Jiang, Qingang Dong.
9: Fair Access to External Memory for Chip-multiprocessors. Shufan Yang, Qiang Wu, Xiongren Xiao, Dominic Hillenbrand, Renfa Li.
10: Self-adaptive heterogeneous cluster with wireless network. Xinyu Niu, Kuen Hung Tsoi, Wayne Luk.

RAW 2012 Program

Tuesday, May 22, 2012

8:00-9:30	IPDPS Opening & IPDPS Keynote
9:30-10:00	Coffee Break
10:00-11:00	**RAW Keynote 2:** Frabrice Lemonnier, THALES Research & Technology - STI Group, France "Heterogeneous Manycore with Self-Adaptive Capabilities and the Corresponding Industrial Needs"
11:00-11:05	Short Break
11:05-11:55	**Session 5 - Applications and Special Purpose Architectures with Reconfigurable Hardware 1**
11:05-11:30	An Optimized Reconfigurable System for Computing the Phylogenetic Likelihood on DNA Data. Simon Berger, Nikolaos Alachiotis, Alexandros Stamatakis.
11:30-11:55	FPGA-based Router Virtualization: A Power Perspective. Thilan Ganegedara, Viktor Prasanna.
11:55-12:20	**Introduction to posters 11-15**
12:20-13:30	Lunch
13:30-15:10	**Session 6 - Applications and Special Purpose Architectures with Reconfigurable Hardware 2**
13:30-13:55	A Reconfigurable High Performance ASIP Engine for Image Signal Processing. Hsuan-Chun Liao, Mochamad Asri, Tsuyoshi Isshiki.
13:55-14:20	Area-Efficient FPGA Implementation of Quadruple Precision Floating Point Multiplier. Manish Kumar Jaiswal, C.C. Cheung Ray.
14:20-14:45	FPGA Implementation of SRAM-based Ternary Content Addressable Memory. Zahid Ullah, Manish Kumar Jaiswal, Y. C. Chan, Ray. C. C. Cheung.
14:45-15:10	Improved Bioinformatics Processing Unit for Multiple Applications. Pei Liu, Kolin Paul, Ahmed Hemani.
15:10-15:40	**Introduction to posters 16-20**

15:40-16:30	**Session 7 - Poster Session (Posters 11-20) & Coffee break**

16:30-18:10	**Session 8 - Tools for Partially Reconfigurable FPGAs**
16:30-16:55	DGECS: Description Generator forEvolvedCircuits Synthesis. Fabio Cancare, Davide Basilio Bartolini, Matteo Carminati, Donatella Sciuto, Marco Domenico Santambrogio.
16:55-17:20	A Compiler Back-End for Reconfigurable, Mixed-ISA Processors with Clustered Register Files. Timo Stripf, Ralf König, Jürgen Becker.
17:20-17:45	Modeling for Synthesis with System#. Christian Köllner, Francisco Mendoza, Klaus Mueller-Glaser.
17:45-18:10	FPM: A Flexible Programming Model for MPSoC on FPGA. Chao Wang, Li Xi, Xuehai Zhou, Junneng Zhang.

18:10-18:20 **RAW Closing**

Session 7 Posters

11: RIVER: Reconfigurable Pre-Synthesized-Streaming Architecture for Signal Processing on FPGAs. Dominic Hillenbrand, Christian Brugger, Shufan Yang, Tao Jie, Matthias Balzer.
12: Efficient On-line Hardware/Software Task Scheduling for Dynamic Run-time Reconfigurable Systems. Ahmed Al-Wattar, Shawki Areibi, Faycal Saffih.
13: Model-Driven Approach for Automatic Dynamic Partially Reconfigurable IP Customization. Gilberto Ochoa, Ouassila Labbani, El-Bay Bourennane, Phillipe Soulard.
14: Embodied computing: self-adaptation in bio-inspired reconfigurable architectures. Laurent Rodriguez, Benoît Miramond, Bertrand Granado.
15: On dynamic run-time processor pipeline reconfiguration. Carsten Tradowsky, Florian Thoma, Michael Hübner, Jürgen Becker.
16: Pareto Optimal Temporal Partition Methodology for Reconfigurable Architectures Based on Multi-objective Genetic Algorithm. Weiguang Sheng.
17: Hardware Index to Permutation Converter. Jon Butler, Tsutomu Sasao.

18: Mini-Robot's Performance Optimization via Online Reconfiguration and HW/SW Task Scheduling. Gianluca Durelli, Marco Domenico Santambrogio, Federica Cresci, Mario Porrmann, Donatella Sciuto.
19: SMPP: Generic SAT Solver over Reconfigurable Hardware Accelerator. Zhongda Yuan, Yuchun Ma, Jinian Bian.
20: A High-Performance FPGA-Based Implementation of the LZSS Compression Algorithm. Ivan Shcherbakov, Christian Weis, Norbert Wehn.