RAW 2010

Advance Program

Monday, April 19, 2010

8:00-8:45	Registration
8:45-9:00	Chair's Welcome
9:00-10:00	**RAW Keynote - Paula Pingree, NASA Jet Propulsion Laboratory, USA** Advancing NASA's On-Board Processing Capabilities with Reconfigurable FPGA Technologies: Opportunities & Implications
10:00-10:45	Coffee Break

Session 1 Reconfiguration Techniques and Tools Chair: João M. P. Cardoso

10:45-11:10	PATIS: Using Partial Configuration to Improve Static FPGA Design Productivity Tannous Frangieh, Athira Chandrasekharan, Sureshwar Rajagopalan, Yousef Iskander, Stephen Craven and Cameron Patterson
11:10-11:35	Wirelength Driven Floor Placement for FPGA-Based Partial Reconfigurable Systems Alessio Montone, Marco D Santambrogio and Donatella Sciuto
11:35-12:00	Fast dynamic and partial reconfiguration Data Path with low Hardware overhead on Xilinx FPGAs Michael Hübner, Diana Göhringer, Juanjo Noguera and Juergen Becker
12:00-13:30	Lunch

Session 2 Multicore/Multiprocessing Systems Chair: Marco D. Santambrogio

13:30-13:55	A Reconfigurable Architecture for Multicore Systems Annie Avakian, Jon Nafziger, Amayika Panda and Ranga Vemuri
13:55-14:20	A Shared Reconfigurable VLIW Multiprocessor System Fakhar Anjam, Stephan Wong and M. Faisal Nadeem
14:20-14:45	TLP and ILP exploitation through Reconfigurable Multiprocessing System Mateus Rutzig, Felipe Madruga, Marco Antonio Alves, Henrique Cota, Antonio Carlos Beck, Nicolas Maillard, Philippe O. A. Navaux and Luigi Carro
14:45-15:10	CAP-OS: Operating System for Runtime Scheduling, Task Mapping and Resource Management on Reconfigurable Multiprocessor Architectures Diana Göhringer, Michael Hübner, Etienne Nguepi Zeutebouo and Jürgen Becker

15:10-17:00 Coffee Break and Poster Session

Poster Session — Chairs: João M. P. Cardoso and Aravind Dasu

- Flexible IP cores for the k-NN classification problem and their FPGA implementation
  Elias S. Manolakos and Ioannis Stamoulias
- Automatic Mapping of Control-Intensive Kernels onto coarse-grained reconfigurable architecture with speculative execution
  Ganghee Lee, Kyungwook Chang and Kiyoung Choi
- Virtual Area Management: Multitasking on Dynamically Partially Reconfigurable Devices
  Josef Angermeier, Sándor P. Fekete, Tom Kamphans, Nils Schweer and Juergen Teich
- Self-Configurable Architecture for Reusable Systems with Accelerated Relocation Circuit (SCARS-ARC)
  Adarsha Sreeramareddy, Ramachandra Kallam, Aravind Dasu and Ali Akoglu
- Reconfiguration-aware Spectrum Sharing for FPGA based Software Defined Radio
  Hessam Kooti, Eli Bozorgzadeh, Shenghui Liao and Lichun Bao
- Implementation of the Compression Function for Selected SHA-3 Candidates on FPGA
  Ashkan Namin and Anwar Hasan
- Improving application performance with hardware data structures
  Ravikesh Chandra and Oliver Sinnen
- Adaptive Traffic Scheduling Techniques for Mixed Real-Time and Streaming Applications on Reconfigurable Hardware
  Tobias Ziermann and Jürgen Teich
- Reconfigurable Architecture for Mathematical Morphology using Genetic Programming
  Emerson Pedrino and Valentin Roda
- MU Decoders: A Class of Fast and Efficient Configurable Decoders
  Matthew C. Jordan and Ramachandran Vaidyanathan
- Analysis and validation of partially dynamically reconfigurable architecture based on Xilinx FPGAsMarco D Santambrogio, Paolo Roberto Grassi, Davide Candiloro and Donatella Sciuto
- Stack Protection Unit as a step towards securing MPSoCs
  Slobodan Lukovic, Paolo Pezzino and Leandro Fiorin
- Fast Smith-Waterman hardware implementation
  Zubair Nawaz, Huseyin Ekin Sumbul and Koen Bertels

Session 3 System Level Design — Chair: Michael Huebner

17:00-17:25 High-Level Synthesis Techniques for In-Circuit Assertion-Based Verification
John Curreri, Greg Stitt and Alan D. George

17:25-17:50 Support of Cross Calls between a Microprocessor and FPGA in CPU-FPGA Coupling Architecture
Giang Huong and Seon Wook Kim

17:50-18:15 An Architectural Space Exploration Tool for Domain Specific Reconfigurable Computing
Gayatri Mehta and Alex K. Jones

Tuesday, April 20, 2010

8:00-9:30	**IPDPS Keynote**
9:30-10:00	Coffee Break
10:00-11:00	**RAW Keynote - Ivo Bolsens, CTO and a Senior VP at Xilinx Inc., USA** Programming Customized Parallel architectures in FPGA

Session 4 Architectures and Components Chair: R. Vaidyanathan

11:00-11:25	Memory Architecture Template for Fast Block Matching Algorithms on FPGAs Shant Chandrakar, Abraham Clements, Arvind Sudarasanam and Aravind Dasu
11:25-11:50	A Low-Energy Approach for Context Memory in Reconfigurable Systems Thiago Lo, Antonio Carlos Beck, Mateus Rutzig and Luigi Carro
11:50-12:15	Efficient Floating-Point Logarithm Unit For FPGAs Nikolaos Alachiotis and Alexandros Stamatakis
12:15-13:45	Lunch

Session 4 Applications and Acceleration Engines Chair: Eli Bozorgzadeh

13:45-14:10	A Configurable-Hardware Document-Similarity Classifier to Detect Web Attacks Craig Ulmer and Maya Gokhale
14:10-14:35	A Configurable High-Throughput Linear Sorter System Jorge Ortiz and David Andrews
14:35-15:00	Hardware Implementation for Scalable Lookahead Regular Expression Detection Masanori Bando, Nabi Sertac Artan, Nishit Mehta, Yi Guan and H. Jonathan Chao
15:00-15:25	A GPU-Inspired Soft Processor for High-Throughput Acceleration Jeffrey Kingyens and J. Gregory Steffan
15:25-15:40	Closing remarks