Call for Participation

13th Reconfigurable Architectures Workshop

RAW 2006

April 25–26, 2006
Rodos Palace Resort Hotel
Rhodes Island, Greece
www-raw06.itiv.uni-karlsruhe.de

For advanced program registration visit www-raw06.itiv.uni-karlsruhe.de

RAW- Run-Time Reconfiguration & Adaptive Computing: Architectures, Algorithms, Technologie

Final Program

Schedule - Tuesday, April 25th 2006

8.00 - 8.10 **Welcome & Opening**

Jürgen Becker, Universität Karlsruhe (TH), Germany

Serge Vernalde, IMEC, Leuven, Belgium

8.10 - 8.55 **Opening Keynote**

Maya Gokhale, Los Almos National Laboratory, New Mexico

8.55 - 9.55 **Session 1 Hardware Performance Models**

Christoforos Kachris, Stamatis Vassiliadis
Technical University of Delft
Title: “Analysis of a Reconfigurable Network Processor"

Yohei Hasegawa, Shohei Abe, Vu Manh Tuan
Shunsuke Kurotaki, Naohiro Katsura, Takuro Nakamura
Keio University
Title: "Performance and Power Analysis of Time-multiplexed Execution on Dynamically Reconfigurable Processor”

Julio Septién, Hortensia Mecha, Daniel Mozos
Universidad Complutense de Madrid
Jesús Tabero
Instituto Nacional de Técnica Aeroespacial
Title: “2D Defragmentation Heuristics for Hardware Multitasking on Reconfigurable Devices”

9.55 - 10.30 **Coffee-Break**

10.30 - 11.30 **Session 2 Memory Optimization**

Masayasu Suzuki, Yohei Hasegawa, Manh Tuan Vu
Shohei Abe, Hideharu Amano
Keio University
Title: “A Cost-Effective Context Memory Structure for Dynamically Reconfigurable Processors”

Hong-Jip Jung, Zachary Baker, Viktor Prasanna
University of Southern California
Title: “Performance of FPGA Implementation of Bit-split Architecture for Intrusion Detection Systems”

Elena Perez, Javier Resano, Daniel Mozos
Universidad Complutense de Madrid
Franky Catnoor
K.U. Leuven, IMEC
Title: “A configuration memory hierarchy for fast reconfiguration with reduced energy consumption overhead”

11.30 - 12.00 **Session 3 Poster Session**

12.00 - 13.15 **Lunch Break**

13.15 - 14.35 **Session 4 Synthesis Methods**

Markus Rullmann, Renate Merker
Dresden University of Technology
Title: “Maximum Edge Matching for Reconfigurable Computing"

Nicolaus Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier
Motorola, Inc.
Title: “FPGA implementation of a license plate recognition SoC using automatically generated streaming accelerators"

Maik Boden, Steffen Rülke
Branch Lab EAS Dresden
Jürgen Becker
University of Karlsruhe, ITIV
Title: “A High-level Target-precise Model for Designing Reconfigurable HW Tasks”

Gerhard Lienhart, Andreas Kugel, Reinhard Männer
Department for Computer Science V, University of Mannheim
Title: “Rapid Development of High Performance Floating-Point Pipelines for Scientific Simulation”

14.35 - 15.05 **Coffee Break**

15.05 - 16.05 **Session 5 Algorithms and Arithmetics**

Tjerk Bijlsma, Pascal T. Wolkotte, Gerard J.M. Smit
University of Twente
Title: “An Optimal Architecture for a DDC"

Ricardo Chaves, IST/INESC-ID/TUDelft
Georgi Kuzmanov, Stamatis Vassiliadis, TUDelft
Leonel Sousa, IST/INESC-ID
Title: “Reconfigurable Memory Based AES Co-Processor"

Michael Ullmann, Jürgen Becker
University of Karlsruhe, ITIV
Title: “Communication Concept for Adaptive Intelligent Run-Time Systems Supporting Distributed Reconfigurable Embedded Systems"

16.05 - 17.05 **Session 6 Applications and Architecture**

Euripides Sotiriades, Christos Konzanitis, Apostolos Dollas
Technical University of Crete
Title: “FPGA based Architecture of DNA Sequence Comparison and Database Search"

Aditya Kwatra, Viktor Prasanna, Manbir Singh
University of Southern California
Title: “Accelerating DTI Tractography using FPGAs"

Roman Koch, Thilo Pionteck, Carsten Albrecht, Erik Maehle
Institute of Computer Engineering, University of Luebeck
Title: “An Adaptive System-on-Chip for Network Applications"

17.05 - 17.15 **Short Break**

17.15 - 18.35 **Session 7 Dyn. Reconfiguration**

Jens Hagemeyer, Boris Kettelhoit, Mario Porrmann
Heinz Nixdorf Institute
Title: “ Dedicated Module Access in Dynamically Reconfigurable Systems"

Miguel L. Silva, João Canas Ferreira
FEUP/DEEC
Title: “Exploiting dynamic reconfiguration of platform FPGAs: Implementation Issues”

Ronald Hecht, Stephan Kubisch, Harald Michelsen
Elmar Zeeb, Dirk Timmermann
Institute of Applied Microelectronics and Computer Engineering
Title: “A Distributed Object System Approach for Dynamic Reconfiguration”

Michael Huebner, Christian Schuck, Juergen Becker
University of Karlsruhe
Title: “Elementary Block Based 2-Dimensional Dynamic and Partial Reconfiguration for Virtex-II FPGAs”

18.35 **Dinner**

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Schedule - Wednesday, April 26th 2006

9.30 – 10.10 Keynote II

Rainer Hartenstein, TU Kaiserslautern, Germany

Title:"New horizons of very high performance computing (VHPC) - hurdles and chances"

10.10 - 10.30 Coffee Break

10.30 - 11.30 Session 8 Synthesis and Scheduling

Love Singhal, Elaheh Bozorgzadeh
University of California, Irvine
Title: “Physically-aware Exploitation of Component Reuse in Partially Reconfigurable Architectures”

Klaus Danne, Marco Platzner
University of Paderborn
Title: “Partitioned Scheduling of Periodic Real-Time Tasks onto Reconfigurable Hardware”

Yuanqing Guo, Cornelis Hoede, Gerard Smit
University of Twente
Title: “A Pattern Selection Algorithm for Multi-Pattern Scheduling"

11.30 - 12.00 Session 9 Poster Session

12.00 - 13.15 Lunch Break

13.15 - 13.55 Session 10 Performance Driven Applications

Michalis Galanis, Gregory Dimitroulalos, Costas Goutis
University of Patras
Title: “Mapping DSP Applications on Processor Systems with Coarse-Grain Reconfigurable Hardware”

Ricarso Jacobi
Computer Science Department, UNB
Renato Cardoso, Geovany Borges
Electrical Engineering Department, UNB
Title: “VoC: A Reconfigurable Matriz for Stereo Vision Processing”

13.55 - 14.55 Session 11 Reconfigurable Processors

Brian Veale, Sean Jones, John Antonio
School of Computer Science, The University of Oklahoma
Monte Tull
School of Electrical and Computer Engineering, The University of Oklahoma
Title: “Selection of Instruction Set Extensions for an FPGA Embedded Processor Core”

Nick Mould, Monte Tull
School of Electrical and Computer Engineering, The University of Oklahoma
Brian Veale, John Antonio
School of Computer Science, The University of Oklahoma
Title: “Dynamic Configuration Steering for a Reconfigurable Superscalar Processor"

Shobana Padmanabhan, Ron Cytron
John Lockwood, Roger Chamberlain
Washington University in St. Louis
Title"Application-specific Automatic Microarchitecture Reconfiguration"

14.55 - 15.20 Coffee Break

15.20 - 16.20 Session 12 Programming and Applications

Oskar Flordal, Di Wu, Dake Liu
Division of Computer Engineering, ISY, Linköping University
Title: “Configurable CABAC Encoder for Multi-standard Media Compression”

Mohamed Taher, tarek El-Ghazawi
The George Washington University
Title: “Exploiting Processing Locality through Paging Configurations in Multitasked Reconfigurable Systems”

Ciaran Toal, Sakir Sezer
Institute of Communications and Information Technology
Queens University Belfast
Title: “Investigation into Programmability for Layer 2 Protocol Frame Delineation Architectures”

16.20 - 16.40 Short Break

16.40 - 17.40 Session 13 Hardware Architectures

Sebastian Lange, Martin Middendorf
University of Leipzig
Title: “On Multi-level Reconfigurable Architectures"

Kostas Siozios, Dimitrios Soudris, Antonios Thanailakis
University of Thrace, Greece
Title: “Platform-based FPGA Architecture: Designing High-Performance and Low-Power Routing Structure for Realizing DSP Applications

Maryam Mizani, Daler Rakhmatov
University of Victoria
Title: “Pipelined Implementation of 802.11a Physical Layer"

17.40 - 18.00 Closing Remarks

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