12th Reconfigurable Architectures Workshop (RAW 2005)
Program for RAW 2005

Denver, Colorado, USA, Monday - Tuesday

April 4th – 5th 2005

http://www.ece.lsu.edu/vaidy/raw05/

Schedule - Monday, April 4th 2005

8.00 - 8.10: Welcome & Opening

Jürgen Becker, Universität Karlsruhe (TH), Germany
Serge Vernalde, IMEC, Leuven, Belgium

8.10 - 8.55: Opening Keynote

Ivo Bolsens, CTO Xilinx
Xilinx, Inc.; USA
Title: *"FPGAs, the heart of embedded systems"*

8.55 - 9.55: Session 1 Hardware Architectures

Chair: TBD

Weisheng Chong, Masanori Hariyama, Michitaka Kameyama
Tohoku University, Japan
Title: *"Architecture of a Multi-Context FPGA Using Reconfigurable Context Memory"*

Stephan Gatzka, Christian Hochberger
Dresden University of Technology, Germany
Title: *"Hardware Based Online Profiling in AMIDAR processors"*

Minoru Watanabe, Fuminori Kobayashi
Kyushu Institute of Technology, Japan
Title: *"An Optically Differential Reconfigurable Gate Array VLSI chip with a dynamic reconfiguration circuit"*

9.55 - 10.30 Coffee-Break

10.30 - 11.30 Session 2 Applications and Algorithms

Chair: TBD

Mukesh Chugh, Dinesh Bhatia, Poras Balsara
University of Texas at Dallas, USA
Title: *"Design and Implementation of Configurable W-CDMA Rake Receiver Architectures on FPGA"*

Florence Choong Chiao Mei, Mamun Bin Ibne Reaz, Faisal Mohd Yasin
Multimedia University, Malaysia
Title: *"Power Quality Disturbance Detection Using Artificial Intelligence: A Hardware Approach"*

Owen Callanan, Emre Ozer, James Sexton, David Gregg
Trinity College, Dublin, Ireland
Andy Nisbet
Manchester Metropolitan University, Manchester, UK
Title: *"FPGA Implementation of a Lattice Quantum Chromodynamics Algorithm Using Logarithmic Arithmetic"*

11.30 - 12.00 Session 3 Poster Session

Chair: TBD

See Monday Poster Session Schedule
In addition you are invited to take a look at the posters until 6pm.

12.00 - 13.15 Lunch Break

13.15 - 14.35 Session 4 HW/ SW Reconfigurable Systems

Session Chair: TBD

Jingzhao Ou, Viktor K. Prasanna
University of Southern California, USA
Title: *"MATLAB/Simulink Based Hardware/Software Co-Simulation for Designing Using FPGA Configured Soft Processors"*

Michael Huebner, Katarina Paulsson, Juergen Becker
Universität Karlsruhe (TH), Germany
Title: *"Parallel and Flexible Multiprocessor System-On-Chip for Adaptive Automotive Applications based on Xilinx MicroBlaze Soft-Cores"*

Neil Steiner, Peter Athanas
Virginia Tech, USA
Title: *"Hardware-Software Interaction: Preliminary Observations"*

Wim Heirman, Joni Dambre, Jan Van Campenhout
Universiteit Gent, Belgium
Christof Debaes, Hugo Thienpont
Vrije Universiteit Brussel, Belgium
Title: ***"Traffic Temporal Analysis for Reconfigurable Interconnects in Shared-Memory Systems"***

14.35 - 15.05 Coffee Break

15.05 - 16.05 Session 5 Algorithms and Arithmetic

Chair: TBD

Ling Zhuo, Gerald Morris, Viktor Prasanna
EE-Systems, University of Southern California, USA
Title: *"Designing Scalable FPGA-Based Reduction Circuits Using Pipelined Floating-Point Cores"*

Konstantinos Katsoulakis, Tughrul Arslan
School of Engineering and Electronics, University of Edinburgh, UK
Title: *"A Novel Low-Power Reconfigurable Data Path for Advanced Speech Coding Algorithms"*

Pascal Benoit, Lionel Torres, Gilles Sassatelli, Michel Robert, Gaston Cambon
LIRMM, France
Title: *"Automatic Task Scheduling / Loop Unrolling Using Dedicated RTR controllers in Coarse Grain Reconfigurable Architectures"*

16.05 - 17.05 Session 6 Reconfiguration Techniques

Session Chair: TBD

Roozbeh Jafari, Majid Sarrafzadeh
University of California, Los Angeles, USA
Title: *"Quick Reconfiguration in Clustered MicroSequencer"*

Markus Rullmann, Sebastian Siegel, Renate Merker
Dresden University of Technology, Germany
Title: *"Optimization of Reconfiguration Overhead by Algorithmic Transformations and Hardware Matching"*

Heiko Kalte, Gareth Lee
School of Computer Science & Software Engineering, University of Western Australia, Australia
Mario Porrmann, Ulrich Rückert
System and Circuit Technology, University of Paderborn, Germany
Title: *"REPLICA: A Bitstream Manipulation Filter for Module Relocation in Partial Reconfigurable Systems"*

17.05 - 17.15 Short Break

17.15 - 18.15 Session 7 Power Aware Design

Session Chair: TBD

Jawad Khan, Ranga Vemuri
University of Cincinnati, USA
Title: *"Battery-Efficient Task Execution on Reconfigurable Computing Platforms with Multiple Processing Units"*

Michael Ullmann, Wansheng Jin, Juergen Becker
Universität Karlsruhe (TH), Germany
Title: *"Hardware Enhanced Function Allocation Management in Reconfigurable Systems"*

Antonio Carlos Schneider Beck, Luigi Carro
Universidade Federal do Rio Grande do Sul, Brazil
Title: *"Application of Binary Translation to Java Reconfigurable Architectures"*

18.15 Dinner

Schedule - Tuesday, April 5th 2005

8.00 – 9.30 IPDPS Keynote (Plenary Session)

David Culler
University of California, Berkeley

Title: *"Wireless Sensor Networks – Where Parallel and Distributed Processing meets the Real World"*

9.30 – 10.10 Keynote II

Mike Hutton, Principal Engineer Altera
Altera Corp., USA

Title: *"Old and New Challenges in FPGA Architecture Design"*

10.10 - 10.30 Coffee Break

10.30 - 11.30 Session 8 Processor Based Approaches I

Session Chair: TBD

Makoto Okada, Tatsuo Hiramatsu, Hiroshi Nakajima, Makoto Ozone, Katsunori Hirase
Digital Systems Development Center, SANYO Electric Co., Ltd

Shinji Kimura
Graduate School of Information, Production and Systems, Waseda University; Japan

Title: *"A Reconfigurable Processor based on ALU array architecture with limitation on the interconnection"*

Brian Veale, John Antonio
School of Computer Science, University of Oklahoma, USA

Monte Tull
School of Electrical and Computer Engineering, University of Oklahoma, USA

Title: *"Configuration Steering for a Reconfigurable Superscalar Processor"*

Toshiyuki Ito, Junji Kitamichi, Kenichi Kuroda
The University of Aizu, Japan

Yuichi Okuyama
NTT Network Innovation Laboratory

Title: *"A Master-Slave Adaptive Load Distribution Processor Model on PCA"*

11.30 - 12.00 Session 9 Poster Session

Session Chair: TBD

See Tuesday Poster Session Schedule
In addition you are invited to take a look at the posters until 6pm.

12.00 - 13.15 Lunch Break

13.15 - 13.55 Session 10 Processor Based Approaches II

Session Chair: TBD

Razali Jidin, David Andrews, Wesley Peck, Dan Chirpich, Kevin Stout, John Gauch
University of Kansas, USA

Title: *"Evaluation of the Hybrid Multithreading Programming Model Using Image Processing Transforms"*

Remy Eskinazi
University of Pernambuco - Polithecnic School, Brazil

Paulo Maciel, Manoel Eusebio, Paulo Nascimento, Abel Guilhermino, Carlos Valderrama
Federal University of Pernambuco, Brazil

Title: ***"A Timed Petri Net Approach for Pre-Runtime Scheduling in Partial and Dynamic Reconfigurable Systems"***

13.55 - 14.35 Session 11 Network on Chip

Session Chair: TBD

Mateusz Majer, Christophe Bobda, Ali Ahmadinia, Jürgen Teich
University of Erlangen-Nuremberg, Germany

Title: *"Packet Routing in Dynamically Changing Networks on Chip"*

Pascal Wolkotte, Gerard Smit, Gerard Rauwerda, Lodewijk Smit
University of Twente, The Netherlands

Title: *"An Energy-Efficient Reconfigurable Circuit Switched Network-on-Chip"*

14.35 - 15.00 Coffee Break

15.00 - 16.20 Session 12 Acceleration Application

Session Chair: TBD

Michalis Galanis, Athanassios Milidonis, Costas Goutis
University of Patras, Greece

Giorgos Theodoridis
Aristotle University, Greece

Dimitrios Soudris
Democritus University of Thrace, Greece

Title: *"A Framework for Partitioning Computational Intensive Applications in Hybrid Reconfigurable Platforms"*

Melissa Smith, Jeffery Vetter
Oak Ridge National Laboratory, USA

Xuejun Liang
Jackson State University, USA

David Caliga
SRC Computers, USA

Title: *"Accelerating Scientific Applications with the SRC-6E Reconfigurable Computer: Methodologies and Analysis"*

Aravind Dasu, Arvind Sudarsanam
Utah State University, USA

Title: *"High Level - Application Analysis Techniques & Architectures - to Explore Design possibilities for Reduced Reconfiguration Area Overheads in FPGAs executing Compute Intensive Applications"*

Jing Lu, John Lockwood
Washington University in St. Louis, USA

Title: *"IPSec Implementation on Xilinx Virtex-II Pro FPGA and Its Application"*

16.20 - 16.40 Short Break

16.40 - 17.40 Session 13 Memory Architectures

Session Chair: TBD

Ron Sass
University of Kansas, USA

Pradeep Nalabalapu
Ambarella, Inc., USA

Title: *"Bandwidth Management with a Reconfigurable Data Cache"*

Martin Schoeberl
JOP.design

Title: *"Design and Implementation of an Efficient Stack Machine"*

Claudio Mucci, Antonio Deledda, Alberto Fazzi, Mirco Ferri, Massimo Bocchi
ARCES - University of Bologna, Italy

Fabio Campi
Central R&D STMicroelectronics, Italy

Title: *"A Cycle-Accurate ISS for a Dynamically Reconfigurable Processor Architecture"*

17.40 - 18.00 Closing Remarks

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Poster Session Schedule - Monday, April 4th 2005

11.30 - 12.00 Session 3 Poster Session

In addition you are invited to take a look at the posters until 6pm.

Chair: TBD

Gregory Dimitroulakos, Michalis Galanis, Costas Goutis
University of Patras, Greece

Title: *"A Compiler Method for Memory-Conscious Mapping of Applications on Coarse-Grained Reconfigurable Architectures"*

Sajid Baloch, Tughrul Arslan
University of Edinburgh, Scotland UK

Title: *"Domain-Specific Reconfigurable Array Targeting Discrete Wavelet Transform for System-on-Chip Applications"*

Maik Boden, Alex Gleich, Steffen Ruelke
Fraunhofer IIS, EAS Dresden, Germany

Ulrich Nageldinger
Infineon Technologies AG Munich, Germany

Title: *"A Low-Cost Realization of an Adaptable Protocol Processing Unit"*

G. Chen, M. Kandemir
Pennsylvania State University, USA

S. Tosun
Syracuse University, USA

U. Sezer
Dept. of ECE, University of Wisconsin, Madison, USA

Title: *"Reliability-Conscious Process Scheduling under Performance Constraints in FPGA-Based Embedded Systems"*

Christiane Pousa, Luís Góes, Dulcinéia Penha, Carlos Martins
Pontifical Catholic University of Minas Gerais, Brazil

Title: *"Reconfigurable Sequential Consistency Algorithm"*

Lilian Bossuet, Guy Gogniat, Jean-Luc Philippe
Université de Bretagne Sud, France

Title: *"Generic Design Space Exploration for Reconfigurable Architectures"*

Fabrizio Ferrandi, Marco Domenico Santambrogio, Donatella Sciuto,
Politecnico di Milano, Italy

Title: *"A Design Methodology for Dynamic Reconfiguration: The Caronte Architecture."*

Kjetil E. Vistnes, Oddvar Soeraasen
Department of Informatics, University of Oslo, Norway

Title: *"Reconfigurable Address Generators for Stream-Based Computation Implemented on FPGAs"*

Markus Koester, Mario Porrmann, Ulrich Rückert
Heinz Nixdorf Institute / University of Paderborn, Germany

Title: *"Placement-Oriented Modeling of Partially Reconfigurable Architectures"*

João Canas Ferreira, Miguel Magalhães da Silva
FEUP/DEEC and INESC Porto, Portugal

Title: *"Run-time reconfiguration support for FPGAs with embedded CPUs: The hardware layer"*

Kostas Siozios, George Koutroumpezis, Konstantinos Tatas, Dimitrios Soudris, Antonios Thanailakis
Democritus University of Thrace, Greece

Title: *"DAGGER: A Novel Generic Methodology for FPGA Bitstream Generation and its Software Tool Implementation"*

Dennis Bemmann
Humboldt University Berlin, Germany

Title: *"IP Lookup on a Platform FPGA: a Comparative Study"*

Imran Ahmed, Tughrul Arslan
School of Electronics and Engineering. University of Edinburgh, UK

Title: *"Domain Specific Reconfigurable Architecture of Turbo Decoder Optimized for Short Distance Wireless Communication"*

Poster Session Schedule - Tuesday, April 5th 2005

11.30 - 12.00 Session 9 Poster Session

In addition you are invited to take a look at the posters until 6pm.

Chair: TBD

Yasunori Osana, Tomonori Fukushima, Masato Yoshimi, Yow Iwaoka, Hideharu Amano
Keio University, Japan

Akira Funahashi
Kitano Symbiotic Systems Project, ERATO-SORST, Japan Science and Technology Agency, Japan

Title: *"An FPGA-Based, Multi-model Simulation Method for Biochemical Systems"*

Franjo Plavec, Blair Fort, Zvonko G. Vranesic, Stephen D. Brown
University of Toronto, Canada

Title: *"Experiences with Soft-Core Processor Design"*

Matthew Ouellette, Dylan Buli
Xilinx, Inc., USA

Dan Connors
University of Colorado, Boulder, USA

Title: *"Analysis of Hardware Acceleration in Modern Configurable Embedded Systems"*

Evangelos Stefatos, Wei Han, Tughrul Arslan, Robert Thomson
University of Edinburgh, UK

Title: *"Low-Power Reconfigurable VLSI Architecture for the Implementation of FIR Filters"*

Yutian Zhao, Ahmet T. Erdogan, Tughrul Arslan
Institute for System Level Integration, University of Edinburgh, UK

Title: *"A Low-Power Dynamic Reconfigurable FFT Processor"*

Steven Guccione
Cmpware, Inc., USA

Title: *"Programming Configurable Multiprocessors"*

Raymond Peterkin, Dan Ionescu
University of Ottawa, Canada

Title: *"Embedded MPLS Architecture"*

Kolin Paul
Indian Institute of Delhi, India

Title: *"An FPGA based Test Bed for Bio Inspired Computation"*

Heiko Zimmer, Stefan Zink, Thomas Hollstein, Manfred Glesner
FG Mikroelektr. Systeme, TU Darmstadt, Germany

Title: *"Buffer-Architecture Exploration for Routers in a Hierarchical Network-on-Chip"*

Fredy Alexander Rivera Velez, Marcos Sanchez-Elez Martin, Milagros Fernandez Centeno, Roman Hermida Correa
Depto. Arquitectura de Computadores y Automatica - Universidad Complutense de Madrid, Spain

Nader Bagherzadeh
Dept. of Electrical and Computing Engineering, University of California, Irvine, USA

Title: *"Low Power Data Prefetch for 3D Image Applications on Coarse-Grain Reconfigurable Architectures"*

E. Syam Sundar Reddy, Vikram Chandrasekhar, M. Sashikanth, V. Kamakoti Veezhinathan
Indian Institute of Technology Madras, India

Vijaykrishnan Narayanan
Pennsylvania State University, USA.

Title: *"Online Detection and Diagnosis of Multiple Configuration Upsets in LUTs of SRAM-based FPGAs"*

Roland Kasper, Thomas Reinemann, Steffen Toscher
IMAT, University Magdeburg, Germany

Title: *"Dynamic Reconfiguration of Mechatronic Real-Time Systems Based on Configuration State Machines"*