A Polymorphic Hardware Platform

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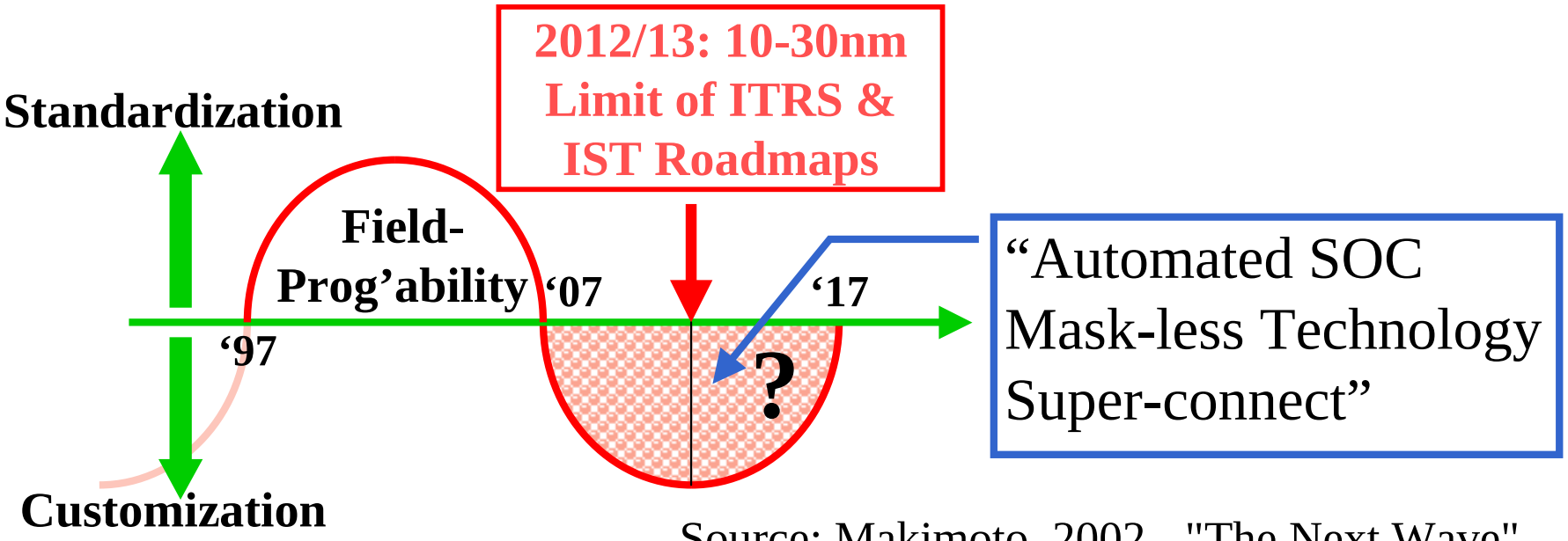
Overview

- The objective
  - Look for new device/architecture opportunities at the nanoscale
- A potential nanoscale device technology
  - Double Gate Transistors
- A 3D reconfigurable building block
  - Based on DG transistors and Resonant Tunneling
- Where is this heading?
  - Reconfigurable *nanocomputer architecture*
- Conclusions

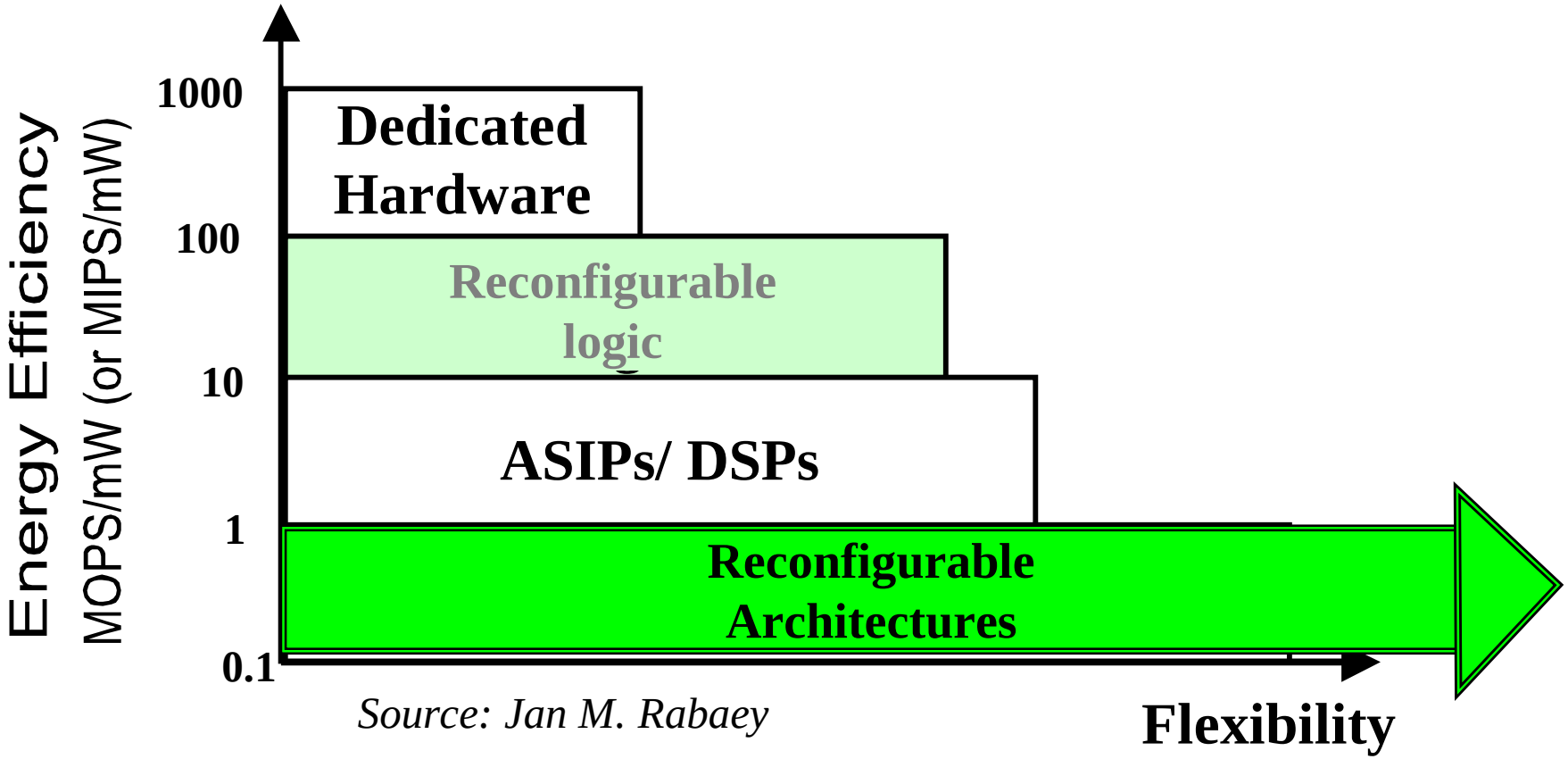
Objective

To explore technologies and architectures for reconfigurable systems that will operate at nanoscale dimensions



Source: Makimoto, 2002 - "The Next Wave"

Reconfigurable/Spatial Architectures

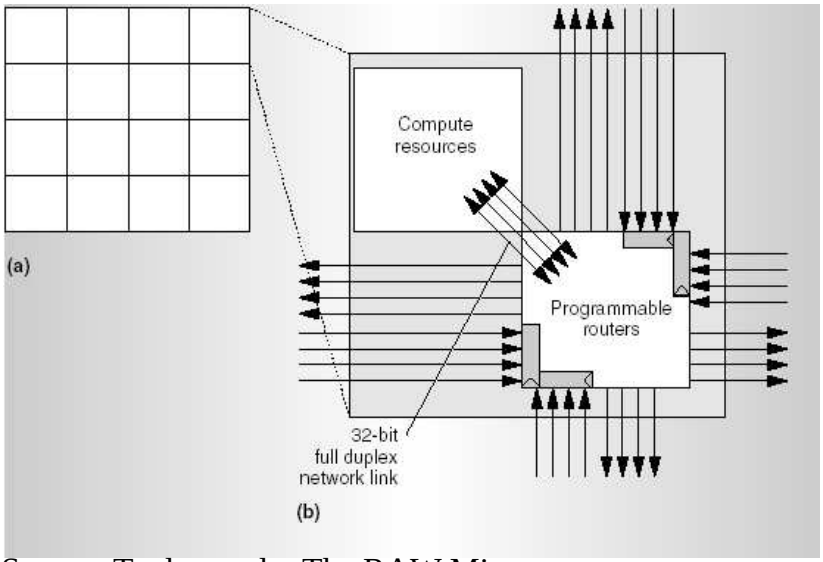


Source: Jan M. Rabaey

Reconfigurable/Spatial Architectures

- simplified processing technology
- flexible organizations
  - allowing a tradeoff between the routing and logic
  - not reliant on global interconnections
- an organization that reduces or hides the overhead imposed by reconfigurability
- high component density

Reconfigurable/Spatial Architectures



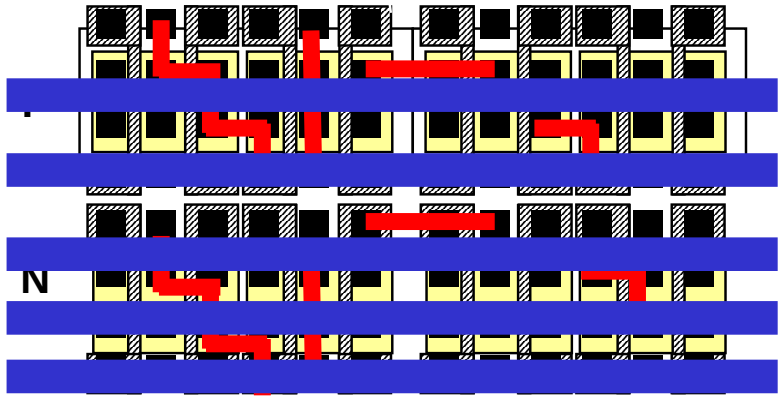
Source: Taylor et al – The RAW Microprocessor

Coarse-grained:

e.g. the RAW Microprocessor

Fine-grained:

e.g. Sea-of-gates



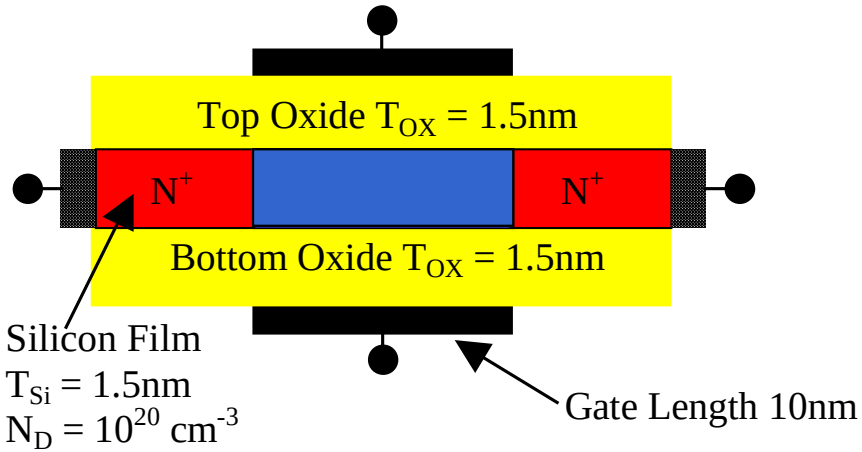
A Nanoscale "Cambrian Explosion"

Disparity →

← Diversity

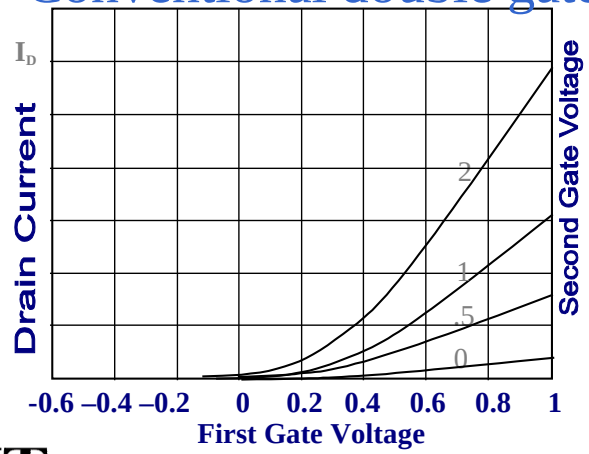
FET (silicon)	Hetero-junction	Nanotube/ Nanowire	Molecular	Magnetic	Quantum-Well
SOI	RTD/ HFET	CNT	Rotaxane	GMR/ CMR	Quantum dot
Si-Ge	RTT logic & memory	C_{60} logic & memory	molecular x-bar	MQCA	Quantum diffraction FET
Double gate	HEMT	Nanotube array logic	CAEN	Hybrid-Hall effect	Quantum interference devices
Vertical FET		Large-bandgap devices (AlN, BN)	Coulomb-coupled optically pumped nanodevices	Molecular nano-magnetics	surface super-lattices
Ballistic nano-FET			DNA	Magnetic RTD	RSFQ
MITT					

Double-Gate MOSFETS

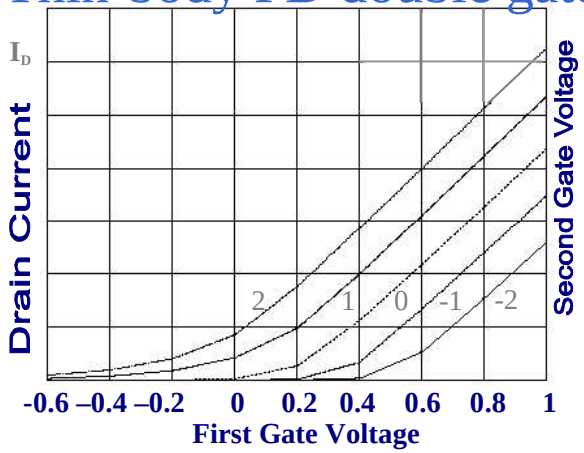


- Thin-body fully depleted MOSFET
  - Gate fields overlap
  - Undoped channel
  - Silicide source/drain alternative to doped silicon
- Variable thresholds

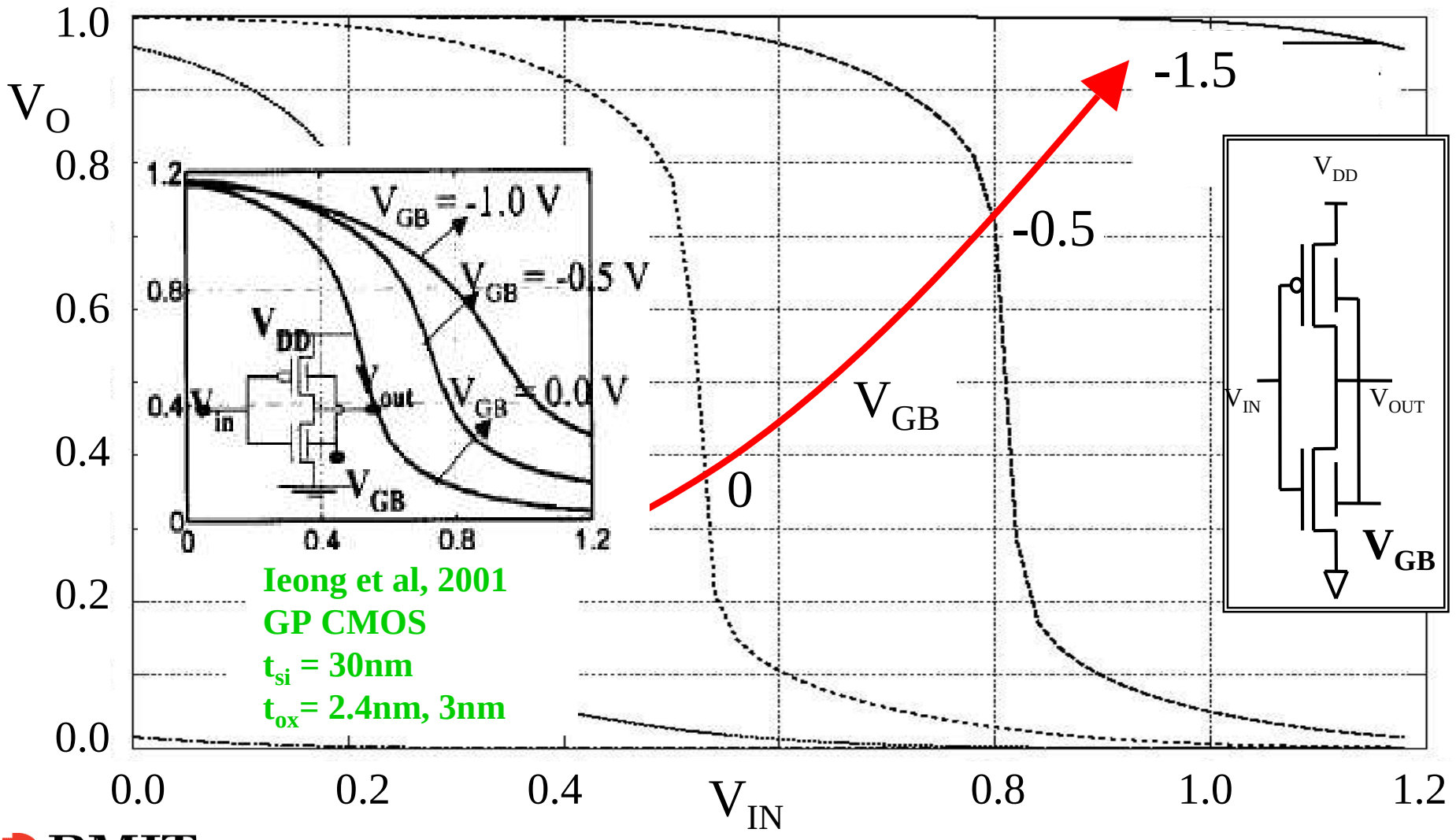
Conventional double gate



Thin-body FD double gate

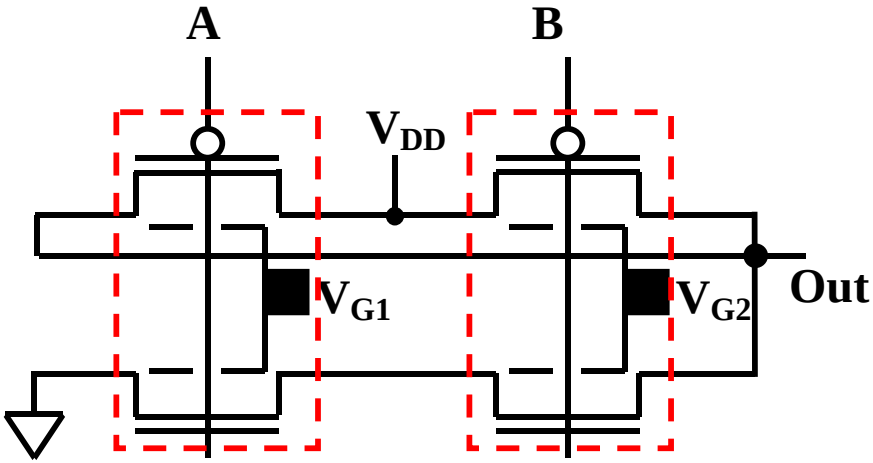


Double-Gate Inverter



A Reconfigurable Logic Cell

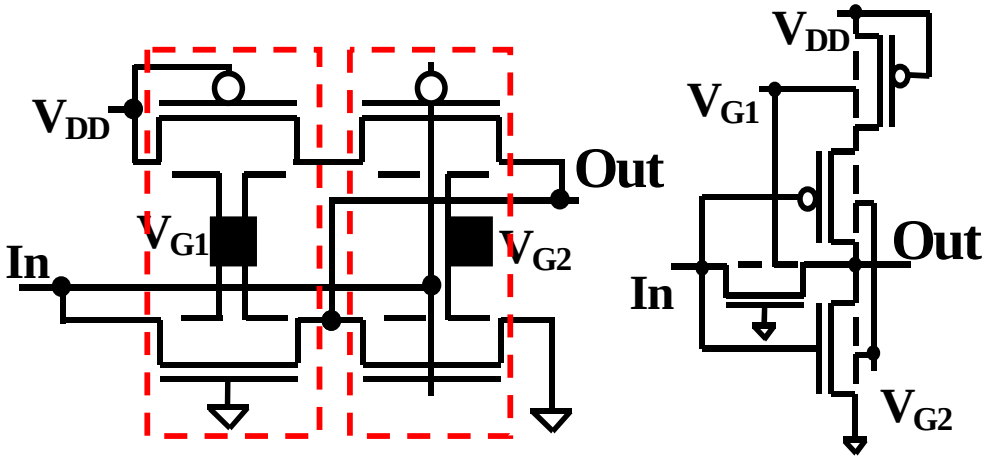
- Simple structure supports complex logic
  - Logic function configured via back gate bias (V_{G1} & V_{G2})
- Locally connected
- Separates logic and configuration planes
- "Polymorphic"?



Fn	V_{G1}	V_{G2}
$\overline{A}$	0	2
$\overline{B}$	2	0
$\overline{A.B}$	0	0
1	-2	-2
0	2	2

A Reconfigurable I/O Cell

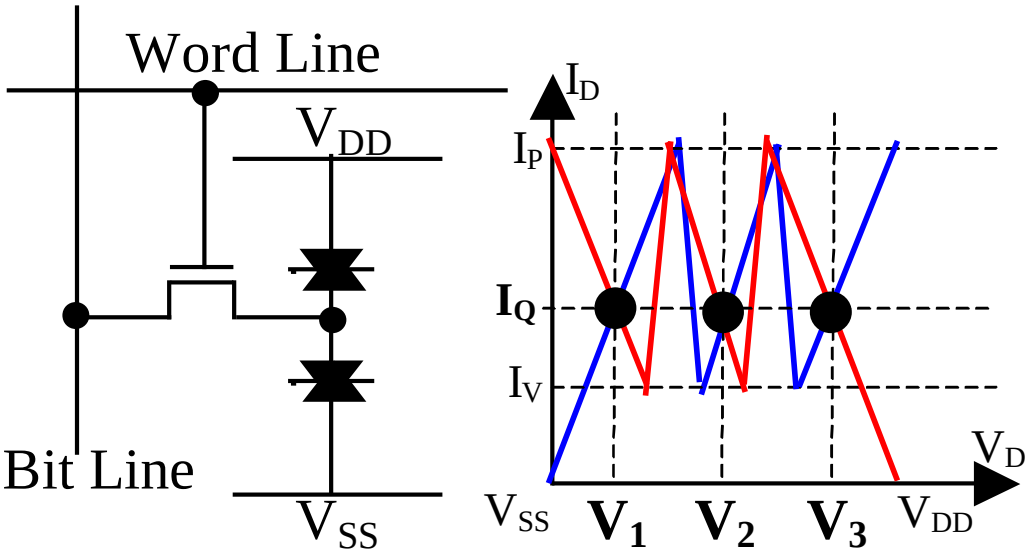
- Inverting/non-inverting 3-state driver
- May be used to determine direction of logic flow

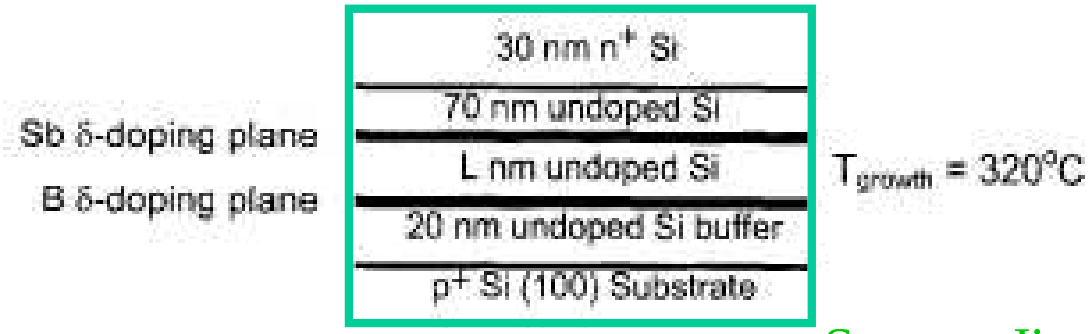


Out	V_{G1}	V_{G2}
$\overline{In}$	-2	0
In	2	-2
Hi-Z	0	-2

Multi-valued SRAM

- 3-state memory (Wei & Lin)
- $V_{1\text{-}3}$ matched by adjusting thickness of RTD barrier layers





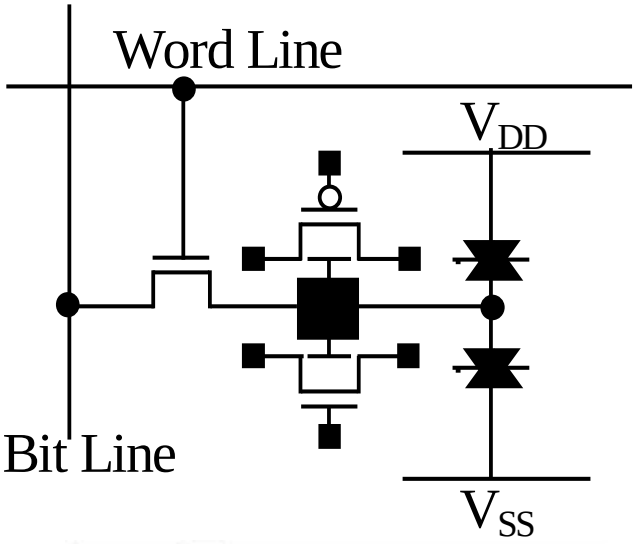
- Ultimate dimensions ≈ 50nm

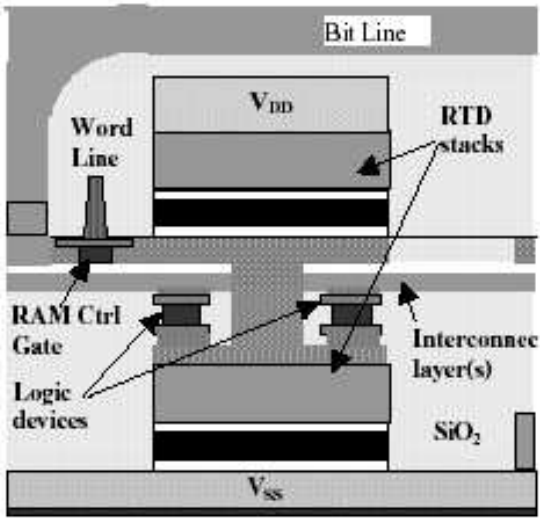
→ ≈ 3 x 10^9 cells/cm^2

Source: Jin et al, 2001

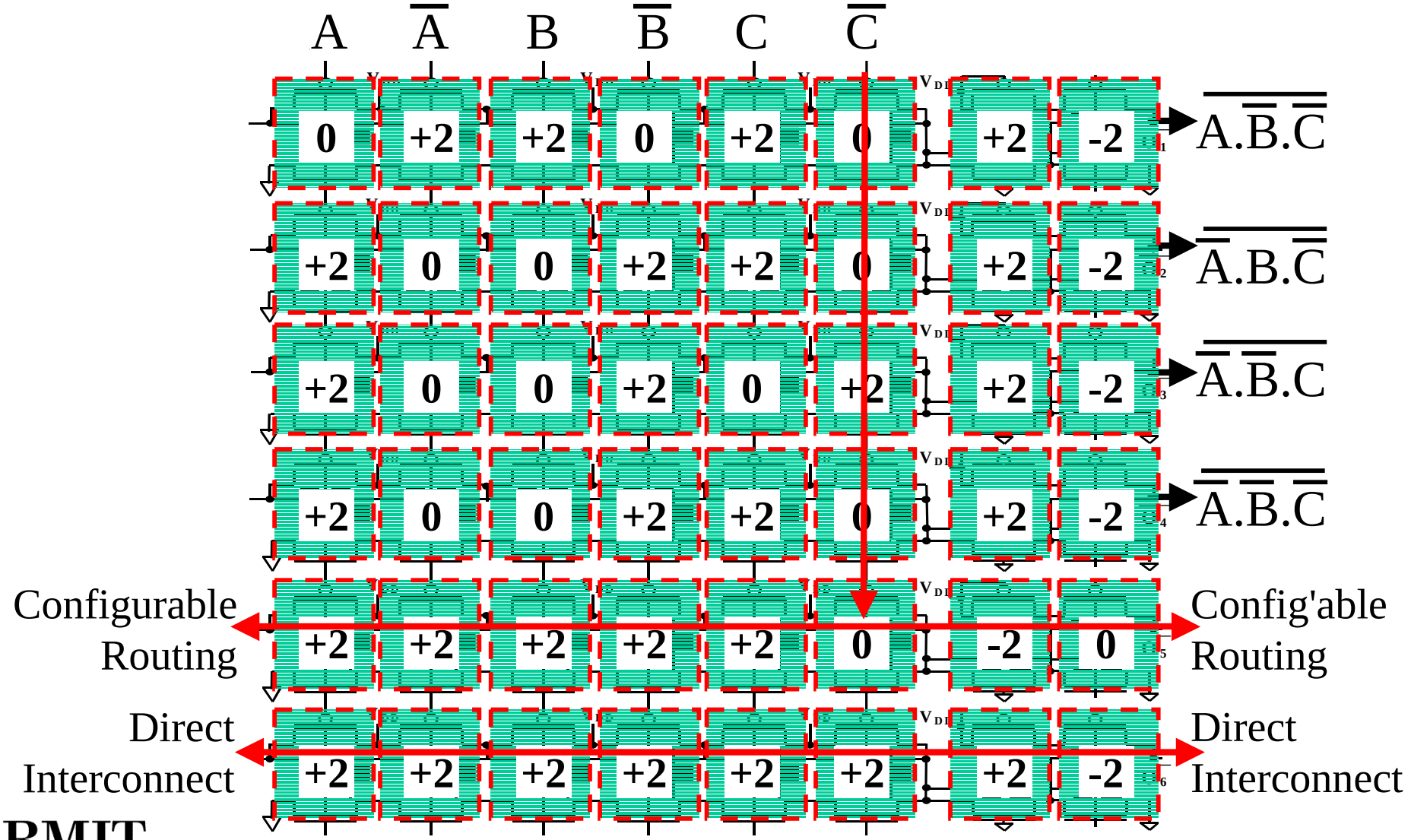
A Reconfigurable Building Block

- Based on 3-transistor cell
- Appears externally as n x m memory array
- Logic complementary pair merged vertically with RTD stack
  - Multivalued storage
  - RTD memory produces configuration bias



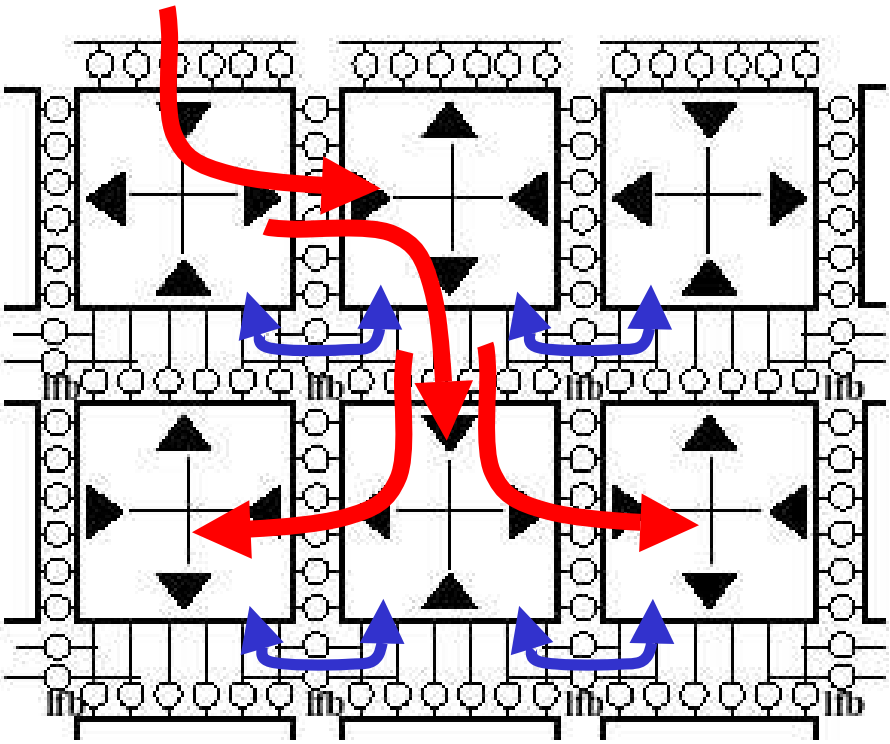


A Reconfigurable Logic Block

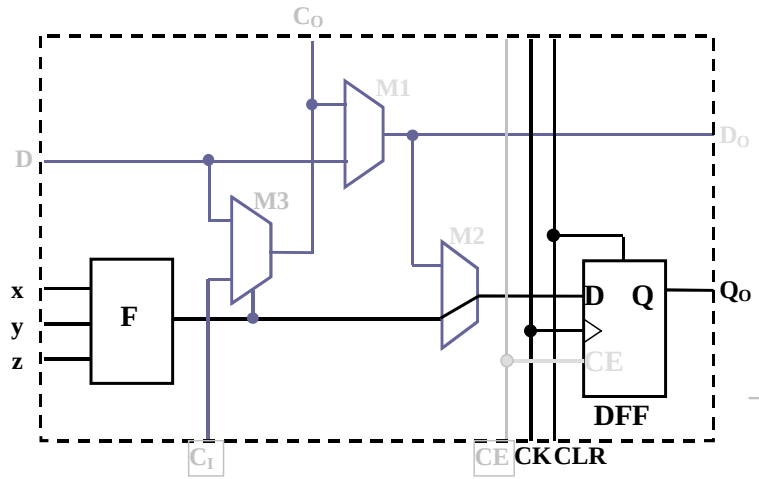


A Polymorphic Array

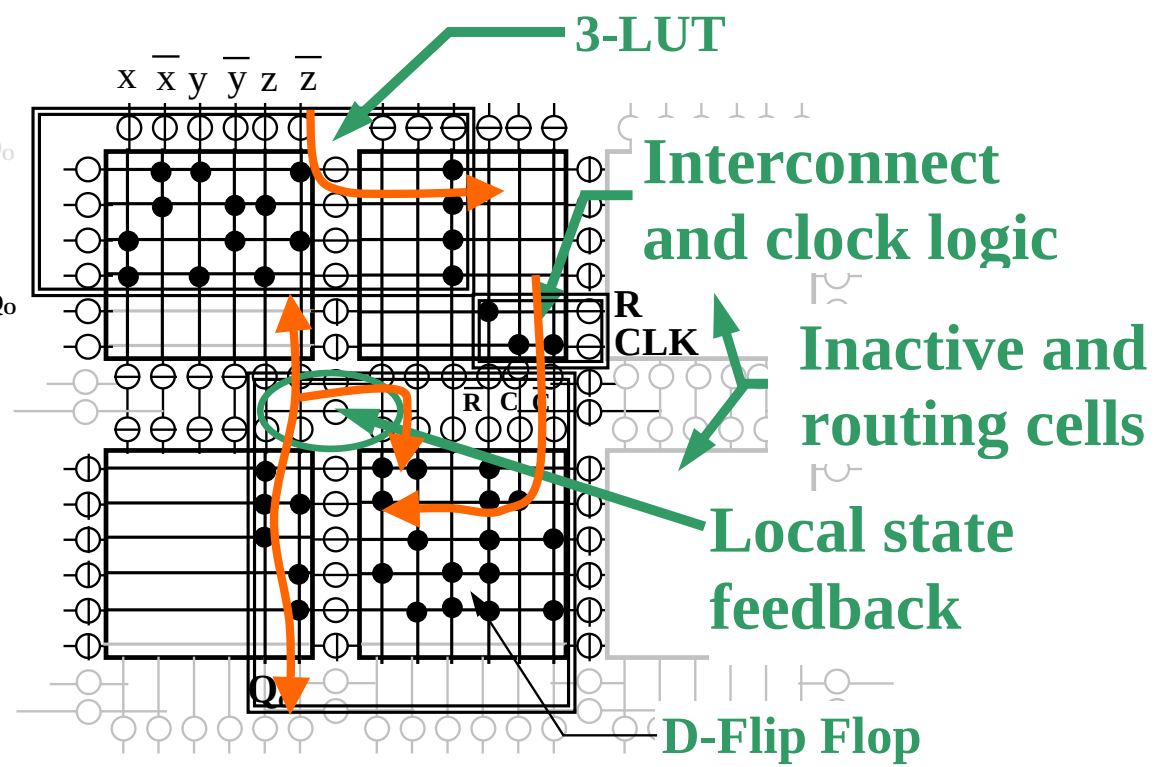
- Logic + I/O cells organized into array with adjacent connections
  - adjacent horizontal and vertical connections
  - local feedback/forward for state, carry chain etc.



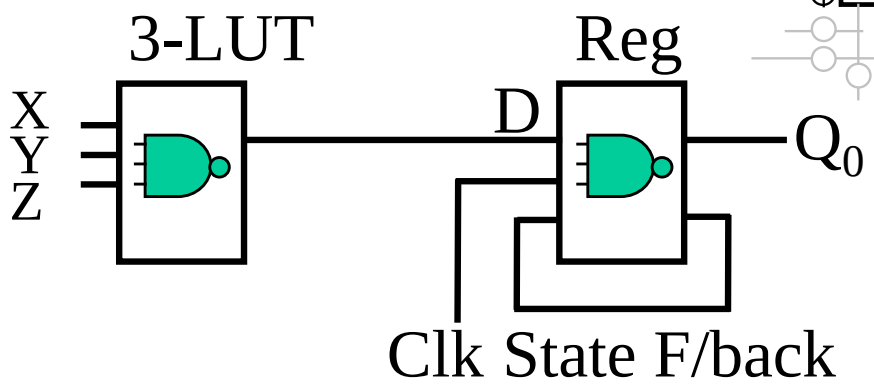
A Polymorphic Array



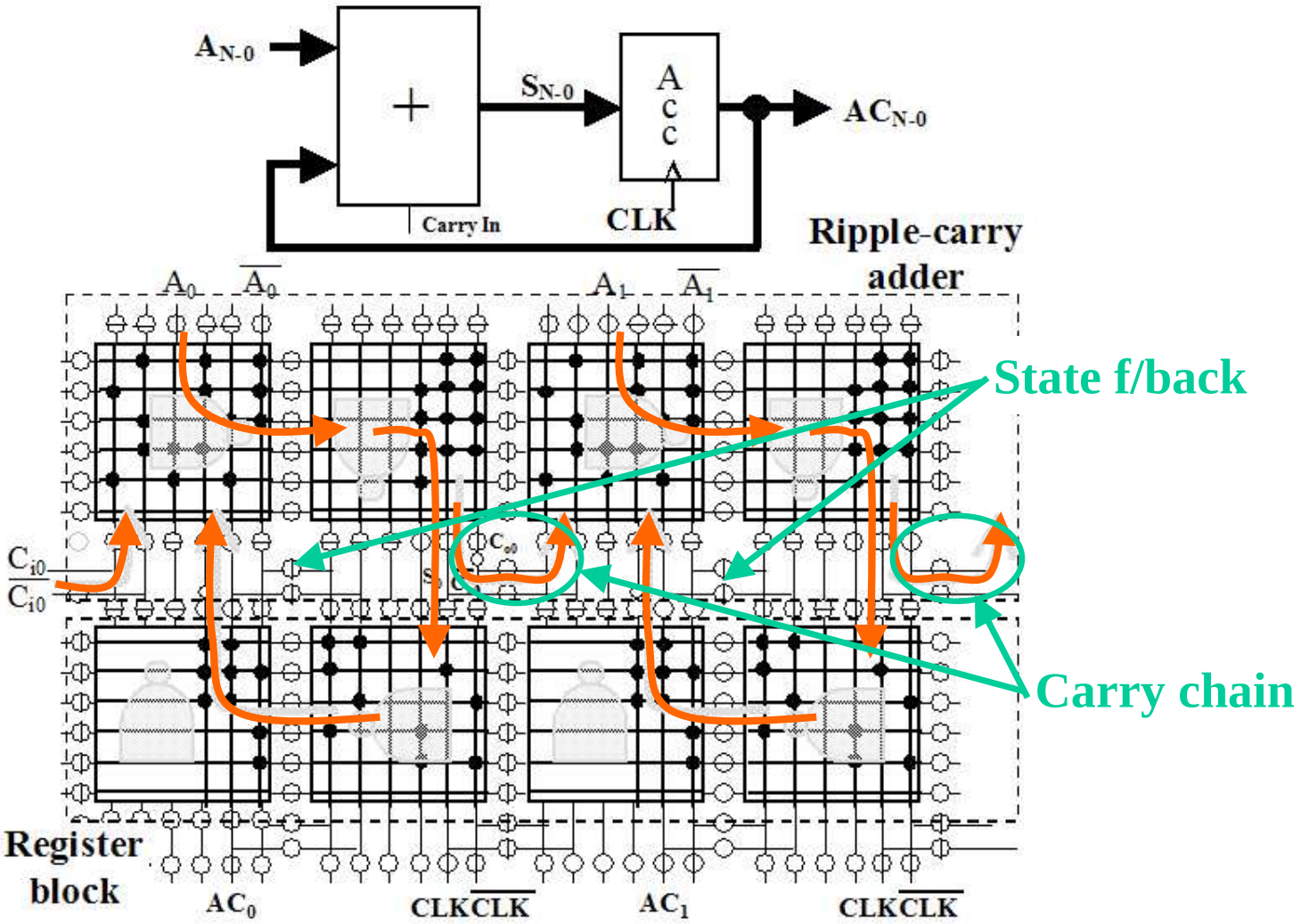
XC5200 CLB



Configured hardware cell

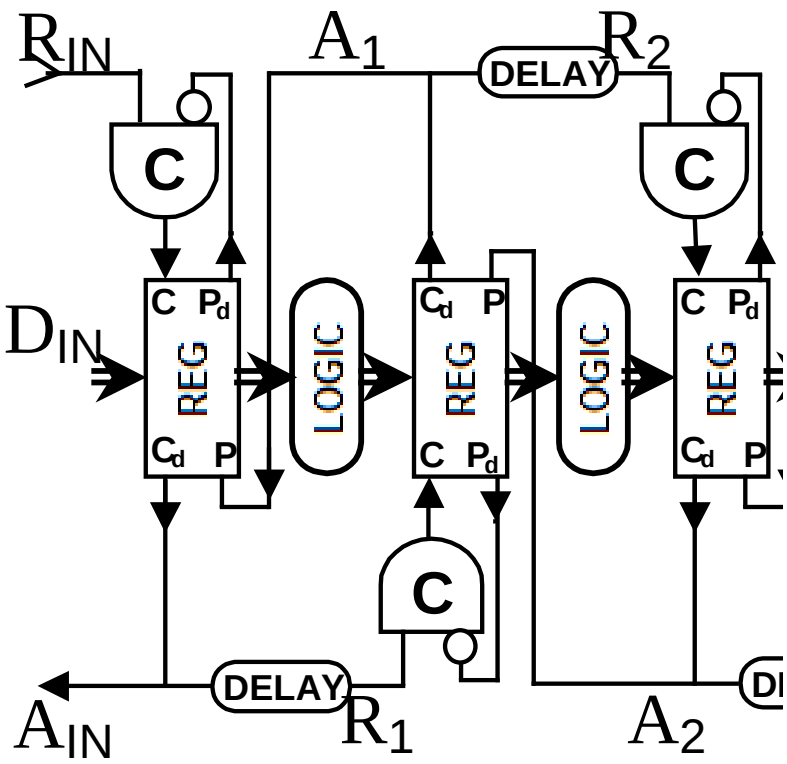


A Polymorphic Array

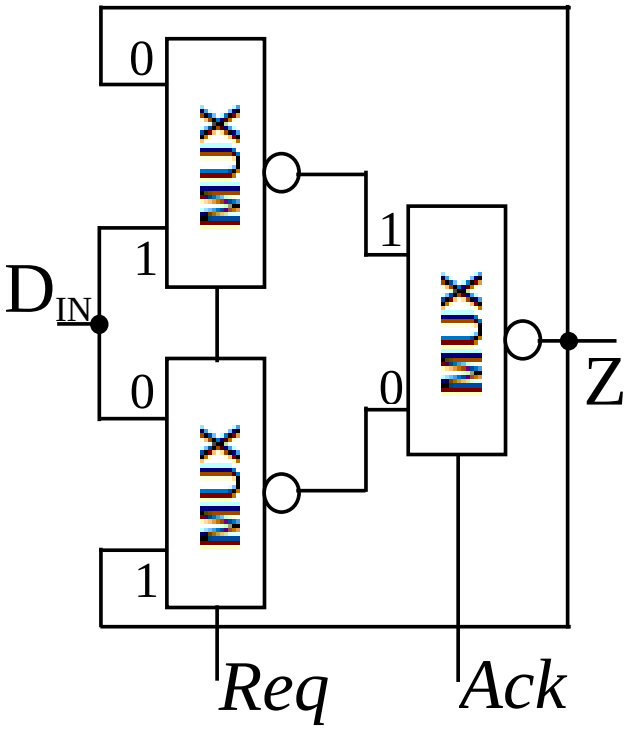


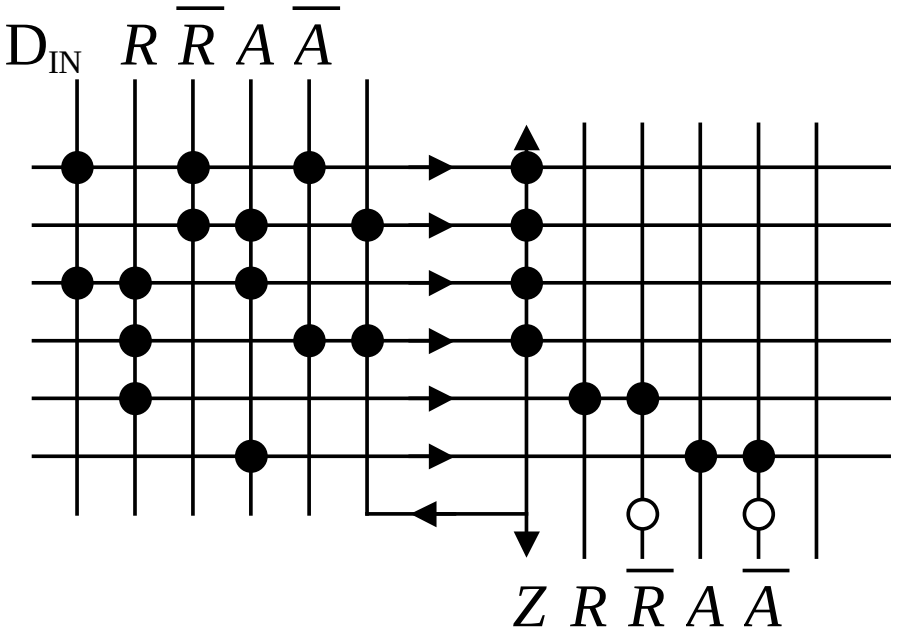
Where to now?

- Reconfigurable Nanocomputer Architectures
- Synchronous (central clock)
  - Power/area?
- Totally asynchronous?
- Globally asynchronous, locally synchronous (GALS)?
- FPGA's not typically suited to asynchronous design
  - MONTAGE, PGA-STC, STACC



Reconfigurable Asynchronous Processing





Event-controlled storage element (Sutherland)

Conclusions

- Future nanoscale components will tend to favor simple, locally connected organizations
  - Complex heterogeneous structures will be increasingly difficult to build
  - Nanoscale devices exhibit poor reliability and low drive
- Nanoscale components can offer novel functionality not available in bulk devices
  - e.g. thin-body undoped SOI processes supports DG transistors with programmable threshold
  - thin film based RTD memory
  - 3D organisations
- Fine-grained reconfigurable architectures will be plausible
  - Need to reduce reconfiguration overheads
  - Need to trade off routing vs. logic
  - Need to use extensive pipelining/ asynchronous design/ GALS

Thank You

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