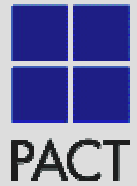
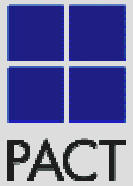

PACT

Today's Mega Trends

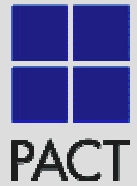


- **Conversion of voice, audio, video & data**
- **Global Mobility**
- **Increasing functionality in devices**
- **Changing standards**
- **Growing barriers of leading edge silicon**

Today's Challenges

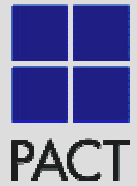


- **Time to market**
- **Development risk**
- **Cost – Cost – Cost**
- **User driven product (2G, 2.5G, WiFi, Games)**
- **Support for multiple standards**
- **Evolving standards in the market**
- **Product life cycle**
- **Market insecurity**



THE solution

Reconfigurable Computing – BUT…



- **Many false starts**
- **Broken promises**
- **No products available**
- **High cost**
- **High efforts (I.e. programming)**

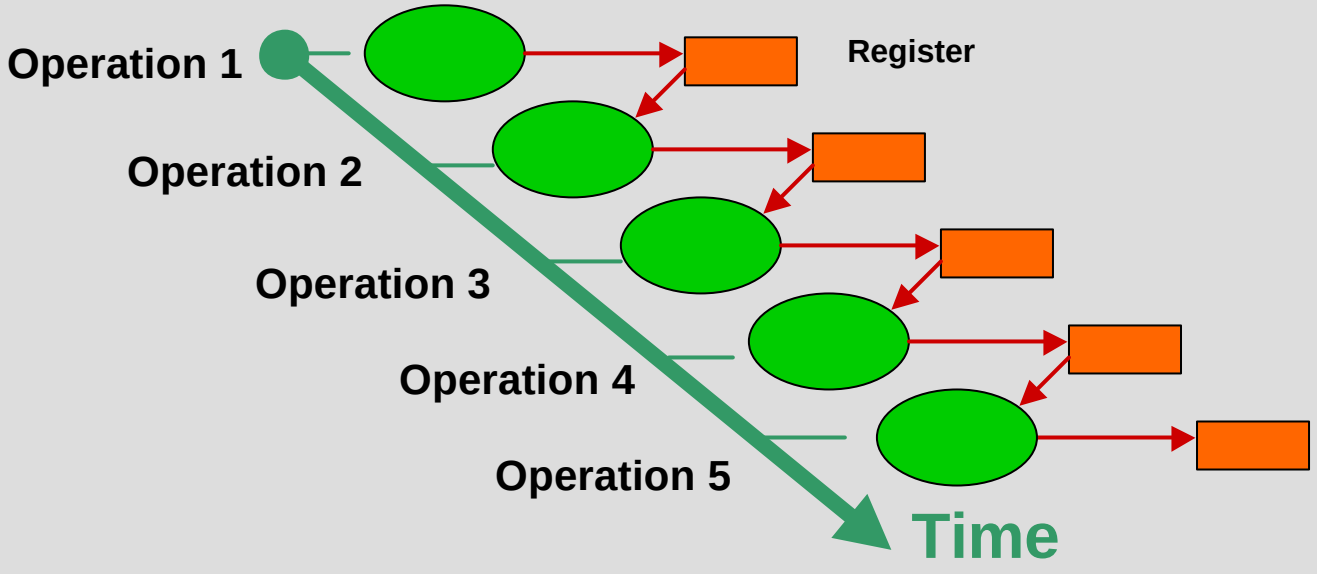
PACT XPP Technology

- **Programmable Hardware Platform**
  - No ASIC NRE cost
  - Low risk
  - Time to market
  - Reusable for multiple products
  - Reusable over multiple generations
- **Standard Software Base & Libraries**
  - Leverage know-how of existing designs
  - Reuse existing code
- **XPP / µP Coupling**
  - Use and leverage 100.000s lines of existing code
  - Easy and cost efficient migration of today‘s code to reconfigurable hardware platforms

PACT XPP Technology

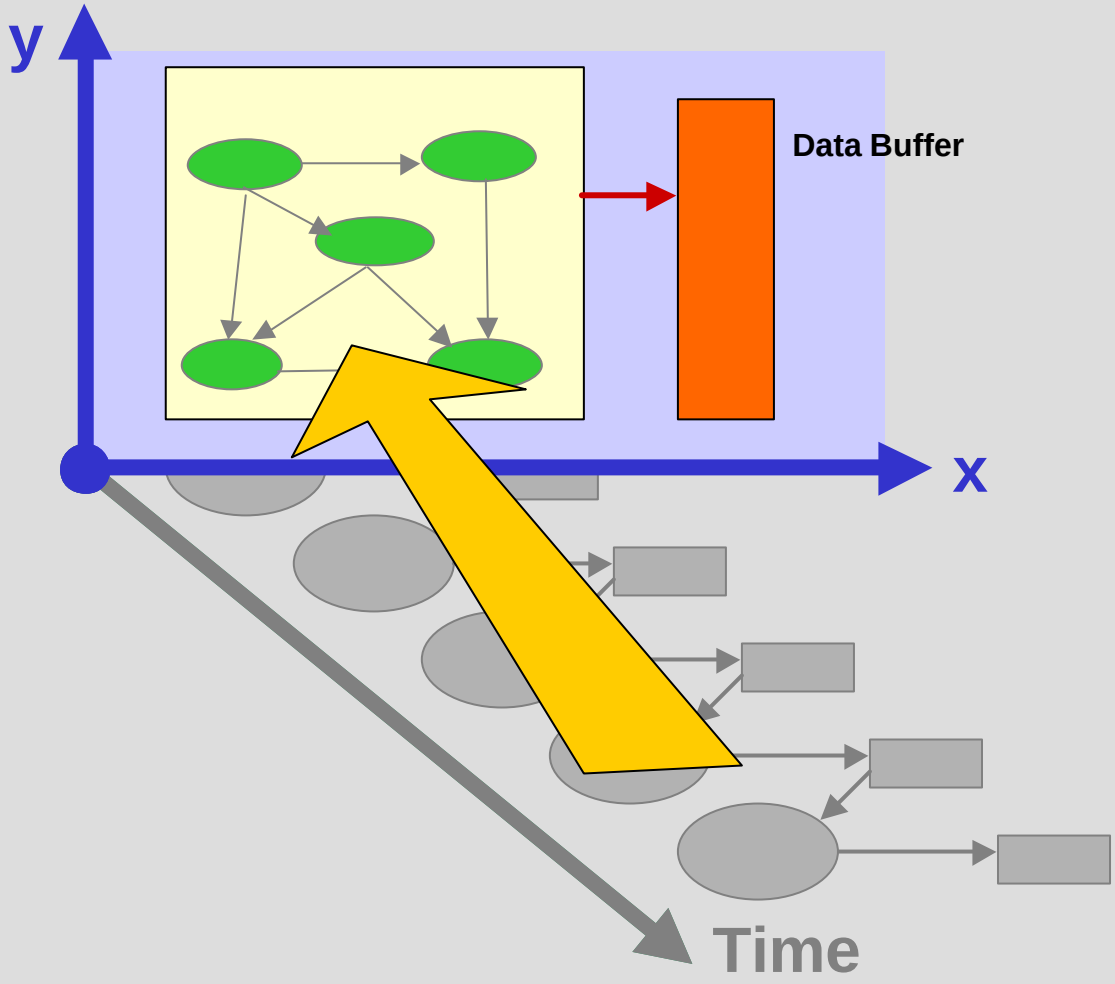
Sequential Processor Model

Conventional processors use the sequential model:
Each operation takes one clock cycle.
Multiple operations are computed consecutively.



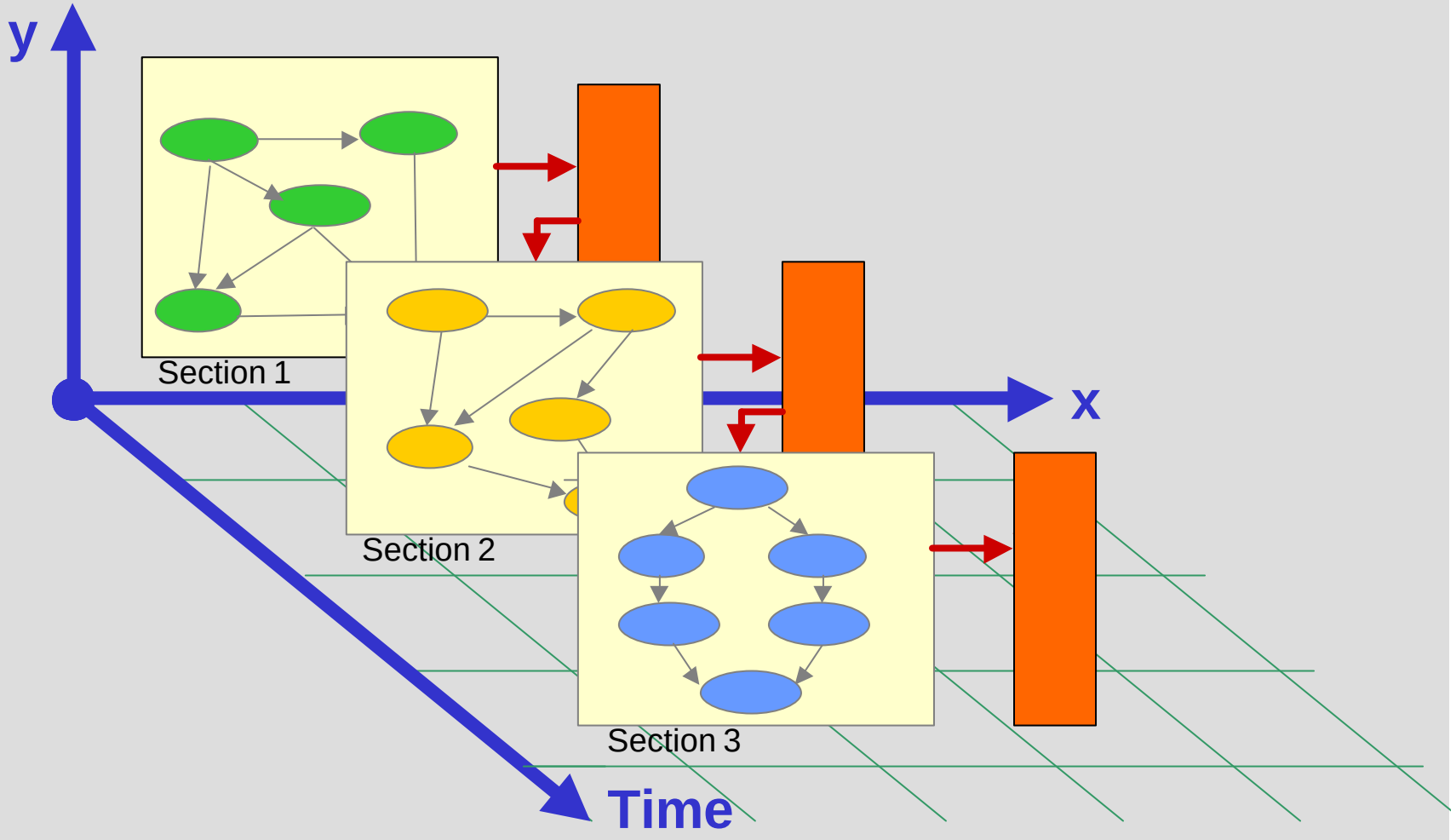
A New Parallel Processor Paradigm

Multiple computations are configured as code sections onto a two dimensional array.

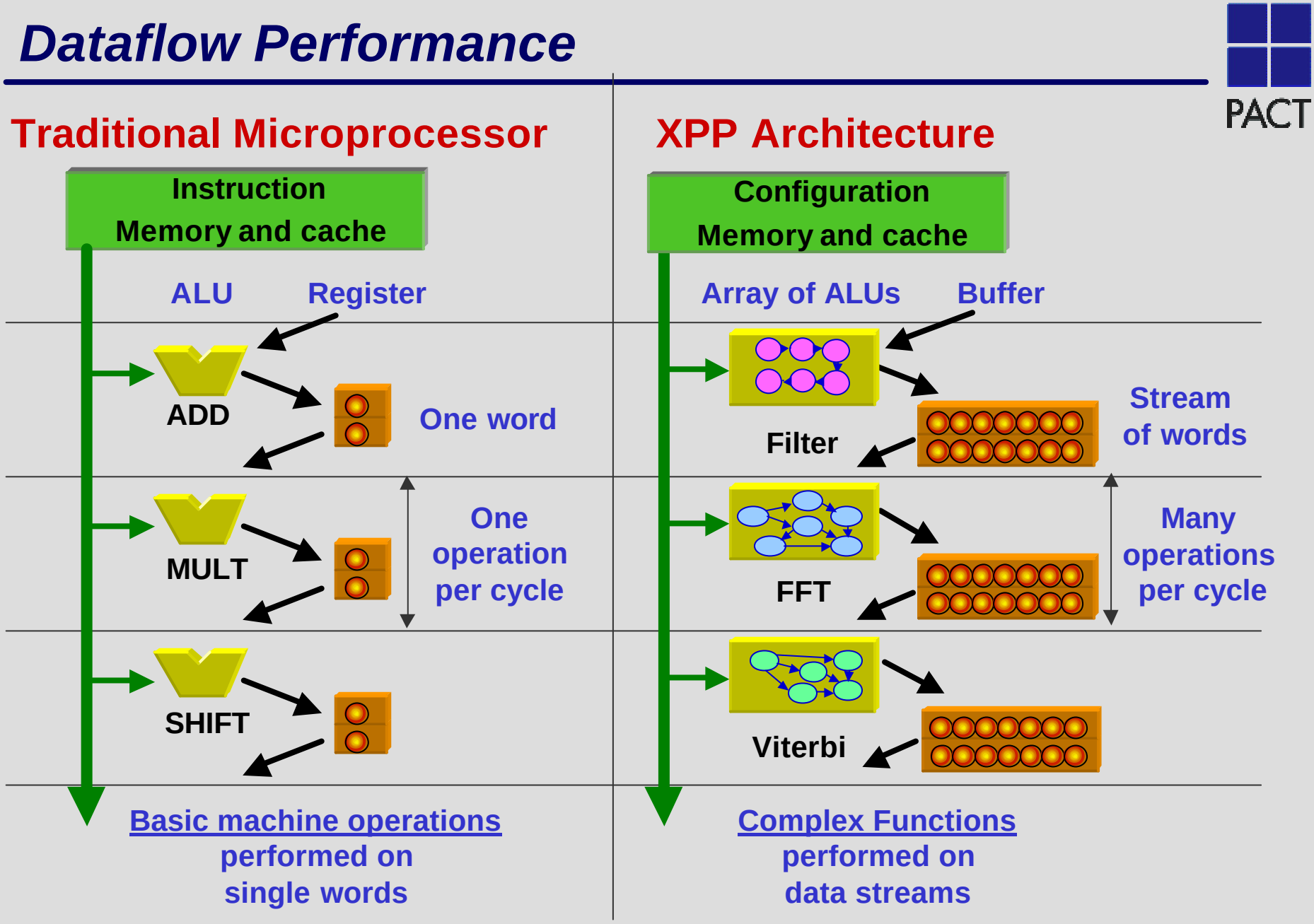


Parallel Processor Model

Multiple code sections are computed sequentially.



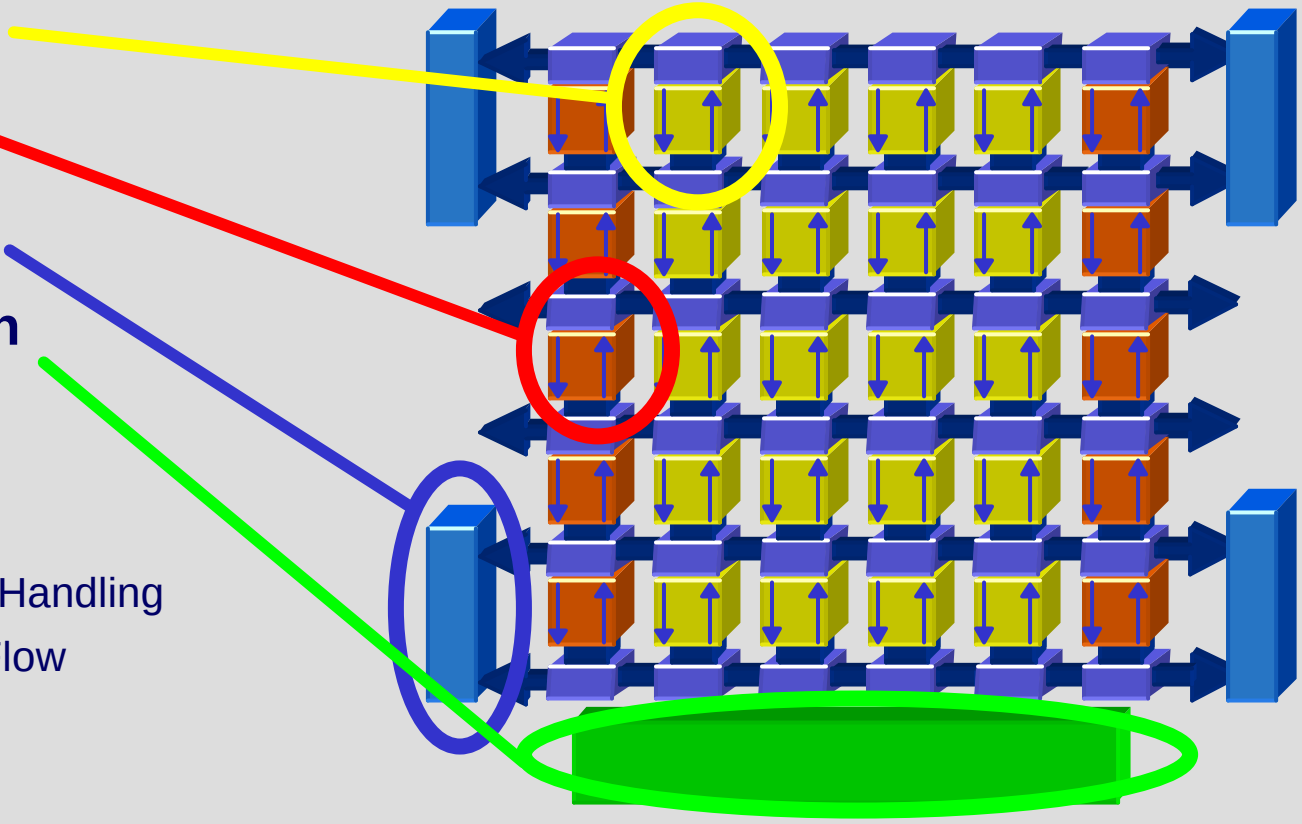
Dataflow Performance



XPP - Modular and Scalable Architecture

XPPs are arrays built from a small number of standardized PAE-elements and are available from 16 to over 100 PAE-elements

- **ALU - PAE**
- **RAM - PAE**
- **I/O-Element**
- **Configuration Manager**

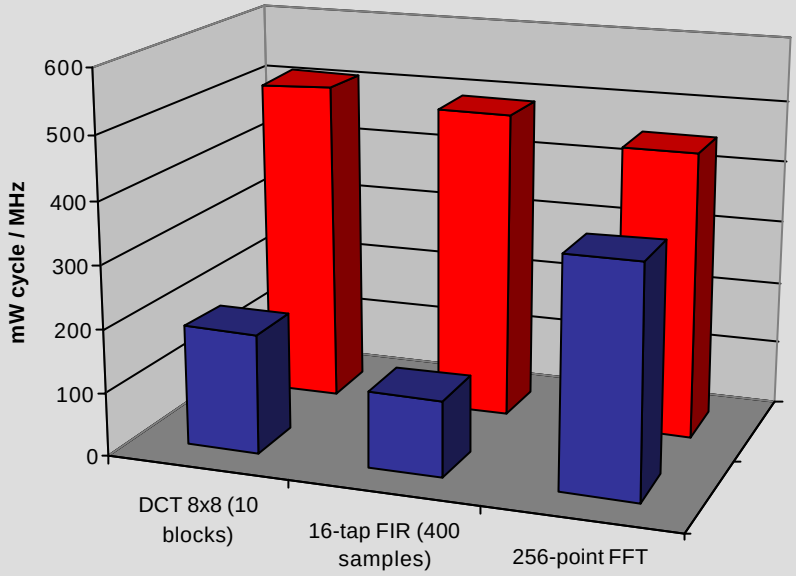


All PAEs include:

- \+ Reconfiguration Handling
- \+ Automatic DataFlow Synchronization
- \+ Event Network

XPP ultra low power technology

Algorithm	XPP16	High End DSP
MPEG Video 2D DCT (8x8)	19 mW cycle / MHz 64 cycles/ block	51 mW cycle / MHz 181 cycles / block
Real 16 Tap FIR Filter (40 Samples)	12 mW cycle / MHz 40 cycles	49 mW cycle / MHz 176 cycles
256-point FFT	360 mW cycle / MHz 1200 cycles	453 mW cycle / MHz 1619 cycles



- XPP16 and High End DSP have equal gate count
- XPP needs less clock frequency due to high parallelism
- XPP has less overhead for:
  - opcode fetch
  - data transfer to register/cache/memory
- Fine grained clock gating per PAE

Applications and Market Segments

Application Example: SMeXPP Multimedia Handset Solution

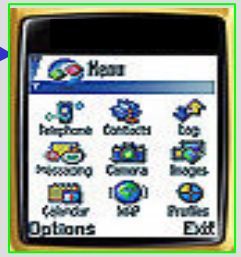
CMOS Camera

CCIR656

I2S

XPP
4x4
System
+ ARM7
EJS

SSC



LCD DISPLAY

BATTERY

ANALOG
AUDIO

DIGITAL
AUDIO

ENERGY
MANAGEMENT

I2S

SSC

UART

SSC

AUDIO I IF
XRAM
YRAM
DSP CORE
PRAM
RFI IF

Baseband Chip

SD/MMC IF
SRAM
BOOT ROM
D CACHE
D TCM
ARM CORE
I CACHE
I TCM
MEM CTR

RX/TX

RF SYSTEM

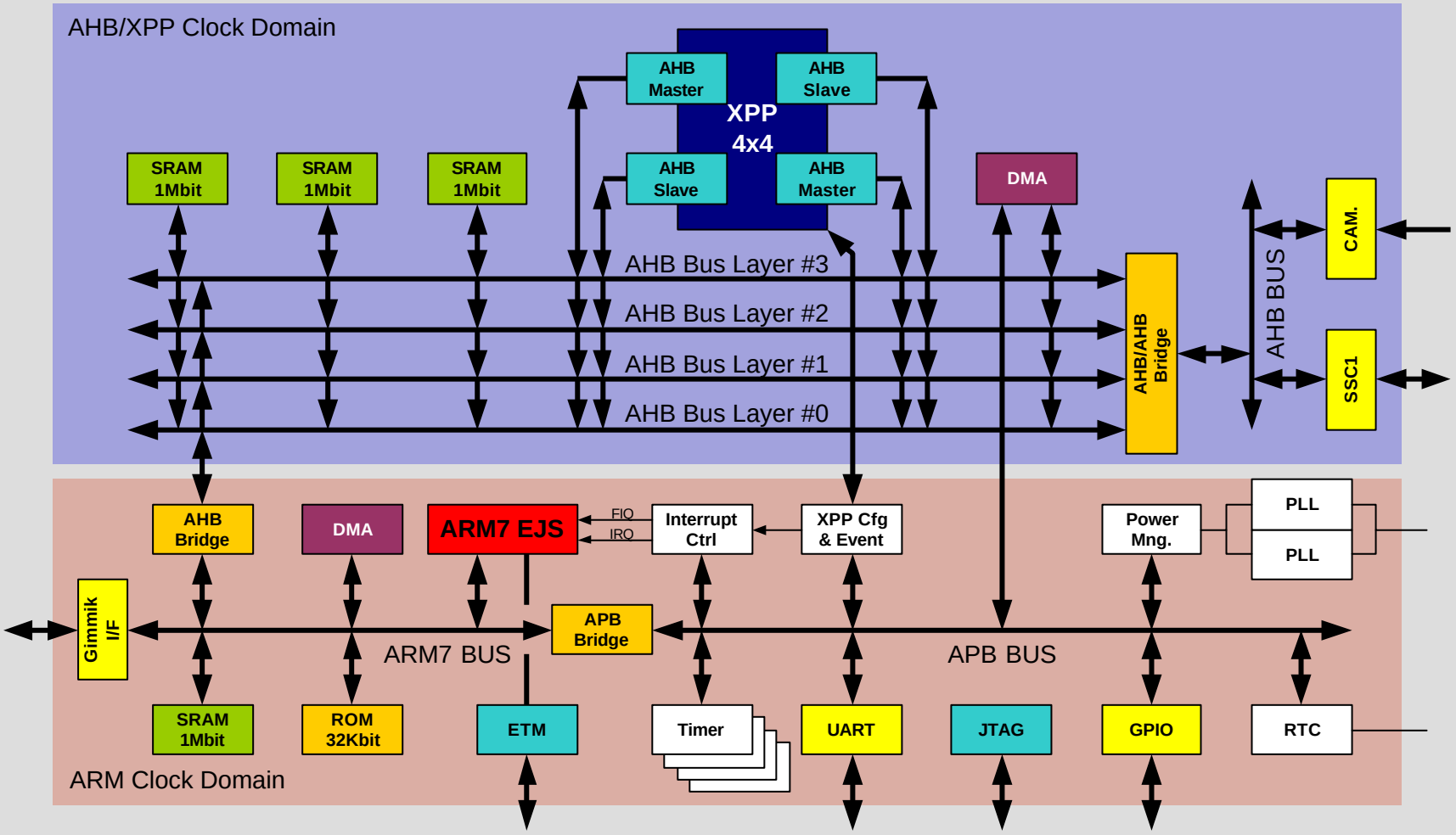
MMC

D / ADR

FLASH / SRAM

SD/MMC

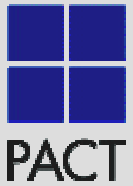
SMeXPP Block Diagram



SMeXPP Technical Benefits

	SMeXPP	Application Processor
Performance	2000 MIPS	500 MIPS
# MACs	16	4
Power	< 0,4 mW/MHz	0,5 – 0,8 mW/MHz
Frequency	13 MHz	208 MHz
Battery Lifetime	> 16x	1x
On Chip Memory	4 MBit	6 MBit
Off Chip Memory	0	16 MB

Application Performance



ARM7+XPP16, 4x4 ALU array, 8 RAM elements:

- **15 fps QCIF MPEG4 Encode @ 13 MHz: < 22 mW**
- **15 fps H.263 Video Conferencing @ 26 MHz: < 60 mW**
- **15 fps CIF MPEG4 Encode @ 52 MHz: < 90 mW**
- **30 fps VGA MPEG4 Encode @ 52 MHz: < 110 mW**

SMeXPP cost : < 10$

SDR / Multimedia – Complete Solution

CMOS SENSOR

CCIR656

Camera I/F

Display I/F

SSC

LCD DISPLAY

Timers

ARM11

Peripherial

PACT
XPP

BATTERY

ANALOG
AUDIO

DIGITAL
AUDIO

ENERGY
MANAGEMENT

I2S

Audio I/F

RF System I/F
GSM
EDGE
CDMA

RX/TX

2.4 GHz
5 GHz
CDMA
GSM
EDGE

internal
memory

SD/MMC

MMC

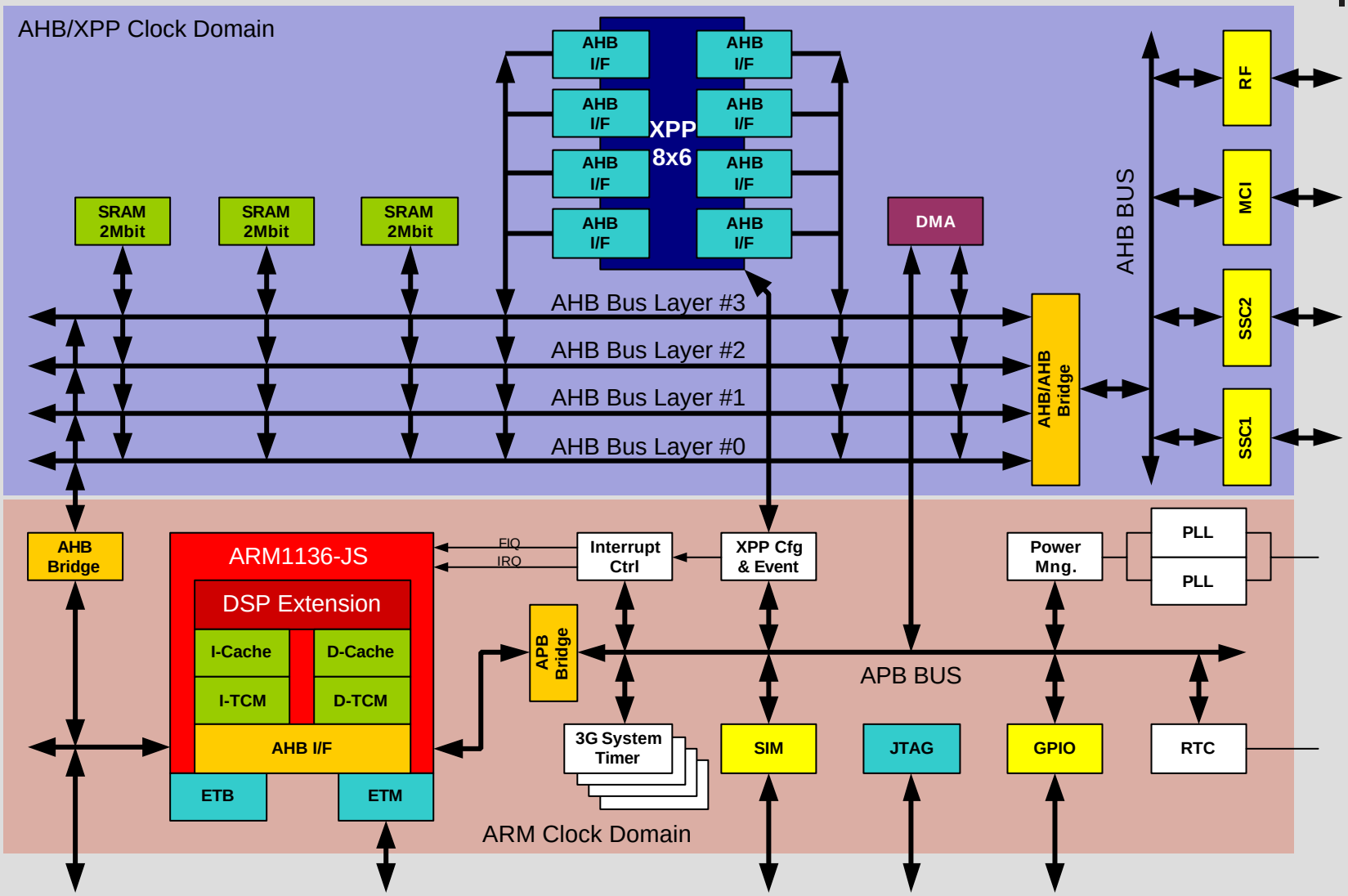
SD/MMC

Memory I/F

D / ADR

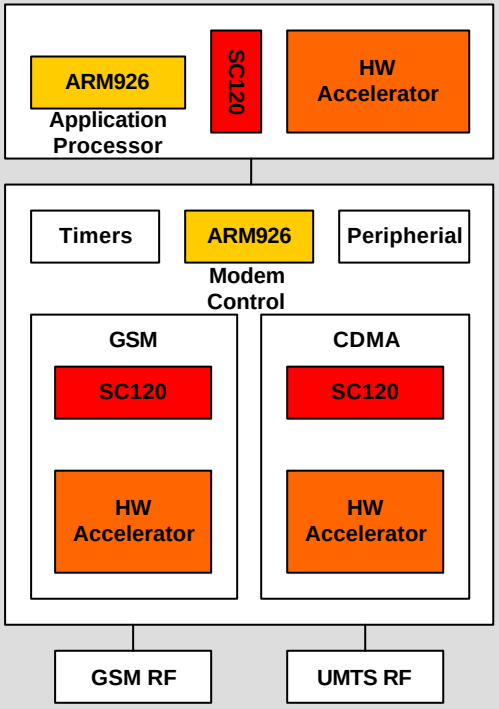
FLASH / SRAM

SdRXPP Block Diagram



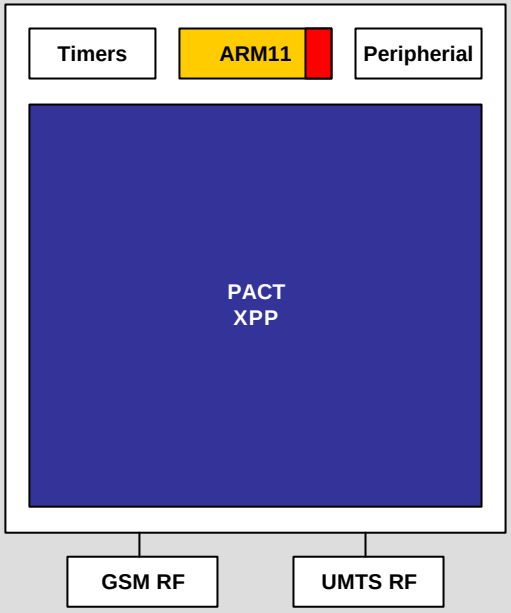
XPP Baseband Solution

Traditional



- **Programming complicated**
  - Multiple µPs/DSPs Communication Debugging
- **Large memory required**
- **Huge die, dual chip solution**
- **Application space limited**
  - Fixed HW accelerators

PACT SDRXPP

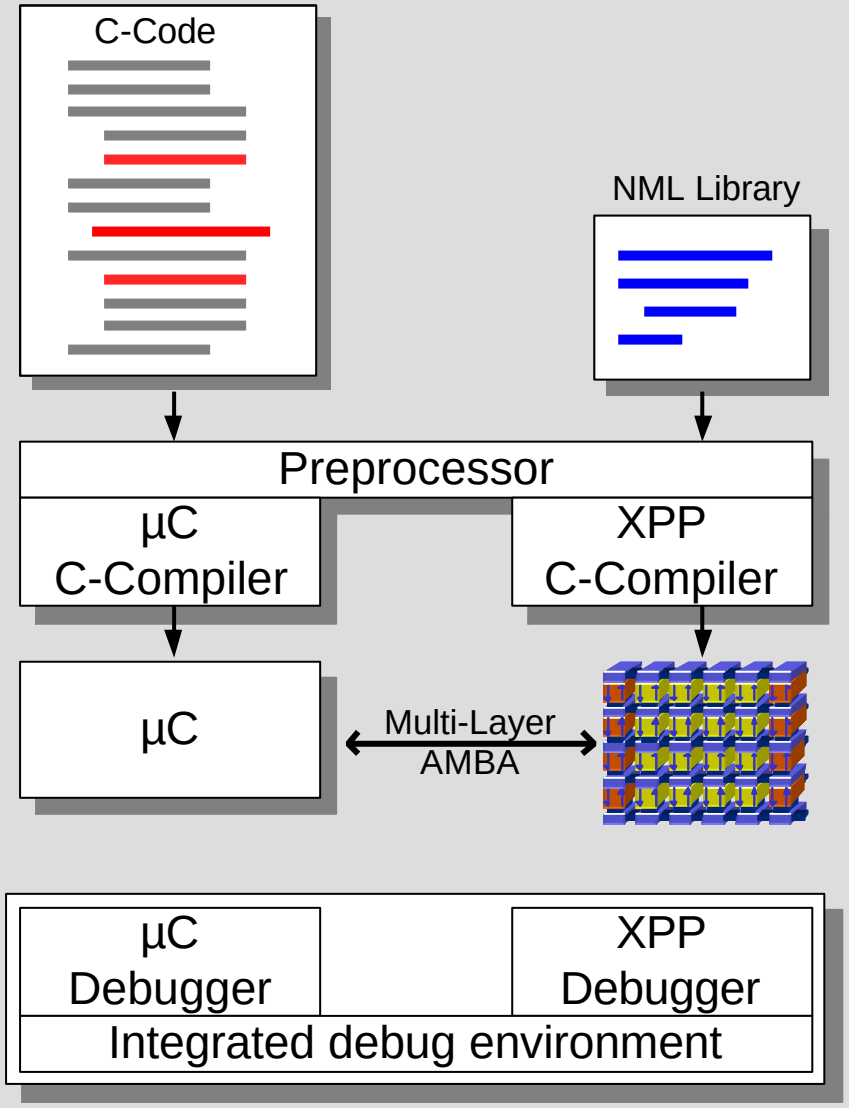


SDRXPP cost : < 25$

- **Easy to program**
  - One master µP + one slave coprocessor
- **Less memory required**
- **Small die, single chip solution**
- **Large application space**
  - Reconfigurable HW accelerator

Software Tools and Programming

XPP integrated C-based tool chain

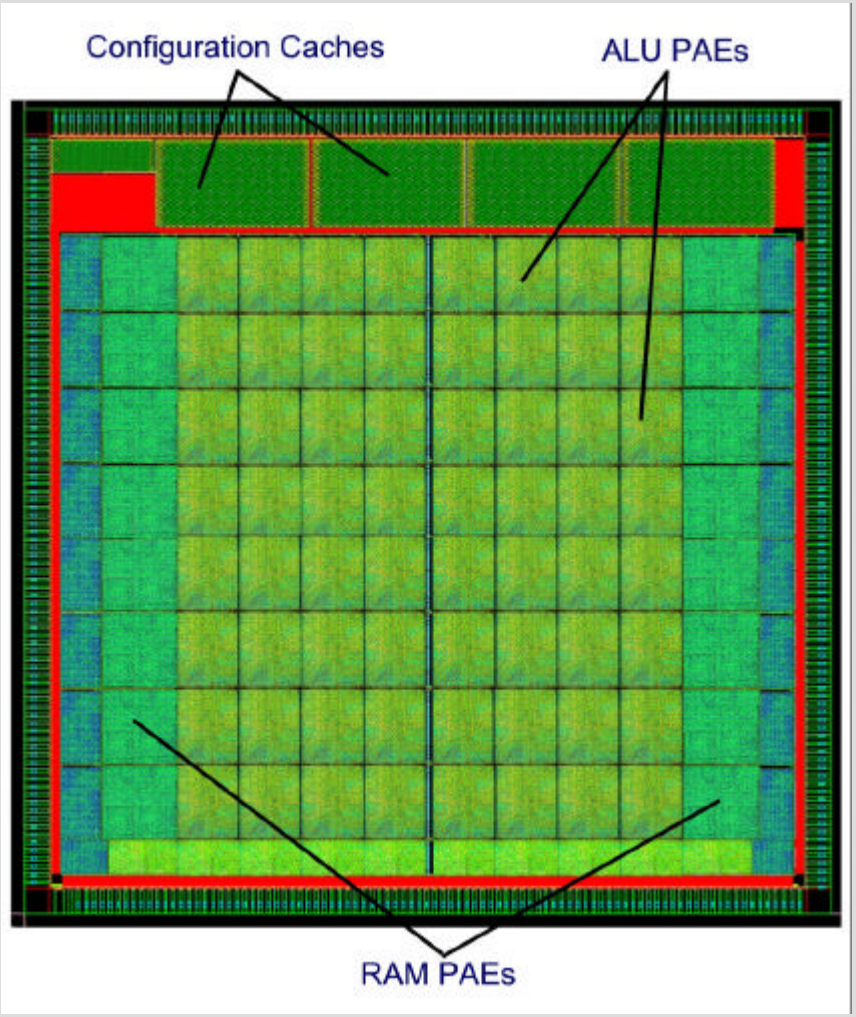


- XPP tools integrated in host processors tools
- One source code for XPP and µC
  - Code exchanged by
    - -Annotation
    - -Library subroutine calls
- Automatic insertion of interface routines for µC and XPP intercommunication
- Integrated debug environment

Silicon Implementation

IP Package

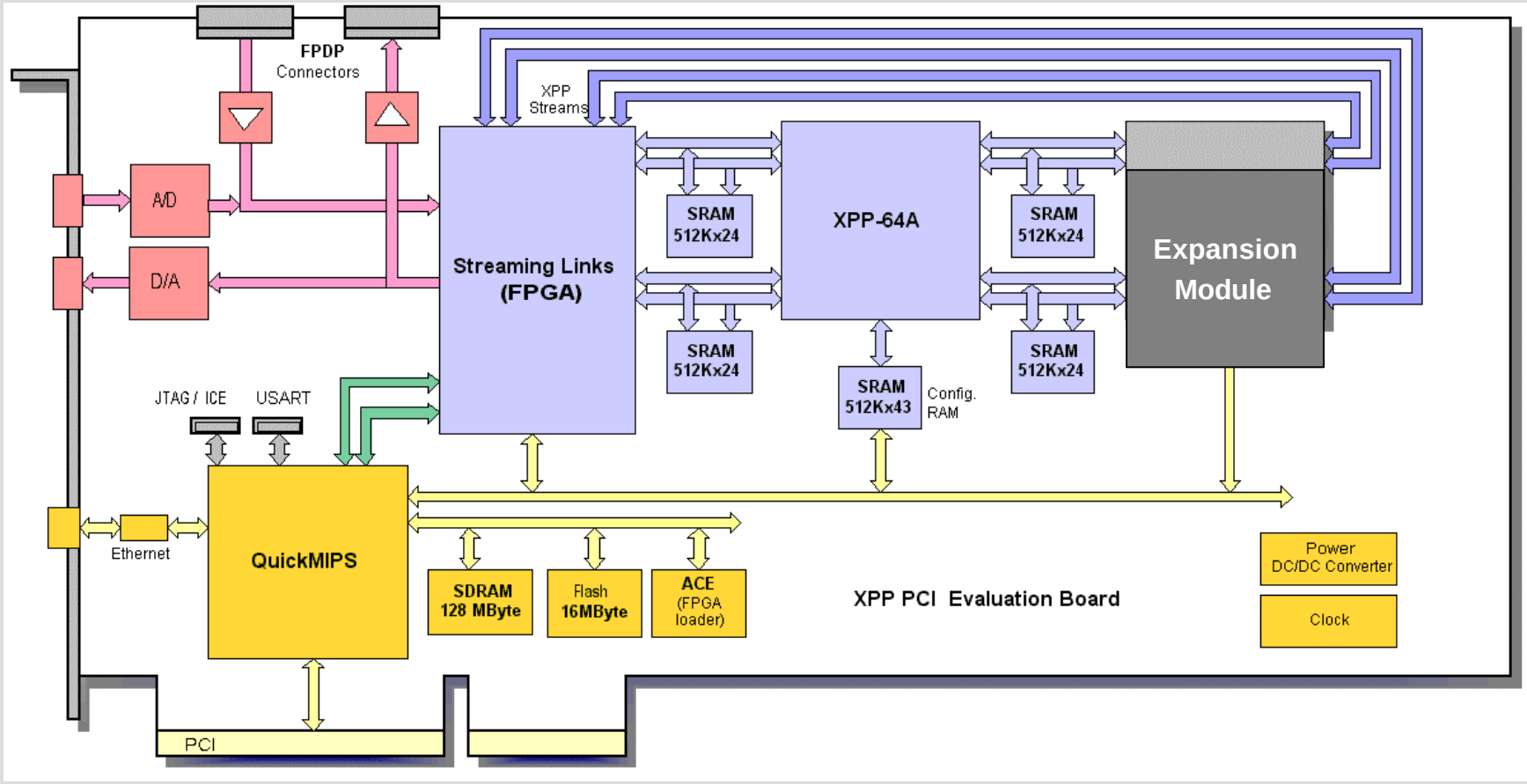
XPP64A Layout & Features



- 64 ALU-PAEs
- 16 RAM-PAEs
- 24-bit architecture
- Split (12,12)-bit opcodes
  - complex addition
  - complex multiplication
  - conditional sign-flip
- JTAG debug interface

- 0.13µ silicon from STMicro, Crolles
- Wafer Out: 03/03/03

XPP64A Development Platform



XPP64 Development Platform & XDS Toolsuite supports evaluation and software development for XPPs arrays in sizes from 16 to 64 elements (i.e. XPP16, XPP32, XPP48)