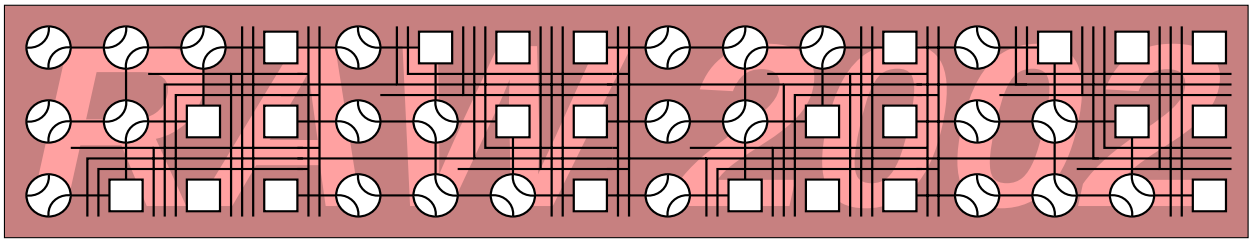
Call For Papers



The 9th Reconfigurable Architectures Workshop (RAW 2002)

Submission Deadline Extended to November 2, 2001

Workshop Web Page: `http://www.ee.lsu.edu/vaidy/raw02/`

The 9th Reconfigurable Architectures Workshop (RAW 2002) is associated with the 16th Annual International Parallel & Distributed Processing Symposium (IPDPS 2002) and is sponsored by the IEEE Computer Society's Technical Committee on Parallel Processing. RAW 2002 is one of the major meetings for researchers to present ideas, results, and on-going research on both theoretical and industrial/practical advances in Reconfigurable Computing.

Main Focus of the Workshop: Run-Time Reconfiguration: Foundations, Algorithms, Tools

Reconfiguration of circuitry at runtime, also called run-time reconfiguration (RTR), is a new dimension in computing that blurs traditional boundaries between hardware and software components. As a consequence, neither the systems architectures nor the hardware/software design methodologies and tools that are available today can fully reveal or exploit the possibilities created by this new computing paradigm. Algorithms and systems designers alike are challenged to harness the potential of innovative devices for the design and application of effective reconfiguration strategies. This goal requires design tools based on robust, formal descriptions of the concepts underlying reconfiguration in order to gain independence from the frequently changing properties of commercially available devices. An appropriate combination of knowledge about the foundations of dynamic reconfiguration, the various models of reconfigurable computing, efficient algorithms, and the tools to support the design and implementation of run-time reconfigurable systems is required. RAW 2002 aims to provide a forum for creative and productive interaction between these disciplines.

Topics of Interest:

Reconfigurable Computing	Systems & Applications	Tools
• Models (R-Mesh, Optical models, etc.) • RTR architectures • Algorithmic techniques • Bounds and complexity issues • Mapping parallel algorithms • Fault tolerance • Configurable resource management	• Devices & reconfiguration techniques • Dynamic instruction set architectures • Adaptive and evolvable hardware • Wireless and distributed systems • Mobile circuitry • Systems support	• High level design methods • Compilation techniques • Virtual machine support • Methodologies and tools

Submission Guidelines: Authors should submit an electronic version of their work for review to Oliver Diessel, University of New South Wales, Australia, (`odiessel@cse.unsw.edu.au`).

All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript (not to exceed 8 pages of single spaced text, including figures and tables), or, in special cases, may be a summary of relevant work. Submissions should be in Postscript (level 2) format. Authors should make sure that the submission can be viewed using ghostscript and will print on a Postscript printer that uses standard letter size paper (8.5" x 11"). Submissions must be received by November 2, 2001.

The IEEE CS Press will publish the IPDPS symposium and workshop abstracts as a printed volume. The complete symposium and workshop proceedings will also be published by IEEE CS Press as a CD-ROM disk.

Important Dates:

Manuscript due	November 2, 2001
Notification of acceptance/rejection	December 5, 2001
Final version due	January 18, 2002

Organization:

- Workshop Chair: Gordon Brebner, University of Edinburgh, UK (gordon@dcs.ed.ac.uk)
- Steering Chair: Viktor K. Prasanna, University of Southern California, USA (prasanna@ganges.usc.edu)
- Program Chair: Oliver Diessel, University of New South Wales, Australia (odiessel@cse.unsw.edu.au)
- Publicity Chair: Ramachandran Vaidyanathan, Louisiana State University, USA (vaidy@ece.lsu.edu)

Program Committee:

- Jeff Arnold, Adaptive Silicon Inc. (USA)
- Peter Athanas, Virginia Tech (USA)
- Gordon Brebner, Univ. Edinburgh (UK)
- Carl Ebeling, Univ. Washington (USA)
- Hossam ElGindy, Univ. New South Wales (Australia)
- Reiner Hartenstein, Univ. Kaiserslautern (Germany)
- Brad Hutchings, Brigham Young Univ. (USA)
- Mohammed Khalid, Quickturn Design Systems (USA)
- Hyoung Joong Kim, Kangwon National Univ. (Korea)
- Rainer Kress, Infineon Technologies (Germany)
- Ron Lin, SUNY Geneseo (USA)
- Wayne Luk, Imperial College (UK)
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- Margaret Marek-Sadowska, Univ. California, Santa Barbara (USA)
- Liam Marnane, Univ. College Cork (Ireland)
- John McHenry, National Security Agency (USA)
- Alessandro Mei, Univ. Rome "La Sapienza" (Italy)
- Martin Middendorf, Univ. Karlsruhe (Germany)
- George Milne, Univ. Western Australia (Australia)
- Koji Nakano, Japan Advanced Inst. of Science & Tech. (Japan)
- Bernard Pottier, Univ. Bretagne Occidentale (France)
- Hartmut Schmeck, Univ. Karlsruhe (Germany)
- Juergen Teich, Univ. Paderborn (Germany)
- Jerry Trahan, Louisiana State Univ. (USA)
- Ramachandran Vaidyanathan, Louisiana State Univ. (USA)
- Peixin Zhong, Lucent (USA)

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