**LSU EE 4755** **Homework 5** **Due: 30 November 2026**

*Formatted 9:09, 23 November 2026*

### Student Expectations

To solve this assignment students are expected to avail themselves of references provided in class and on the Web site, such as for Verilog programming and synthesis examples, and to seek out any additional help and resources that might be needed. (Of course this doesn't mean asking someone else to solve it for you.) It is each student's duty to himself or herself to resolve frustrations and roadblocks quickly. (If you get stuck *just ask for help!*)

This assignment cannot be solved by blindly pasting together parts of past assignments. Solving the assignment is a multi-step learning process that takes effort, but one that also provides the satisfaction of progress and of developing skills and understanding.

### Collaboration Rules

Each student is expected to complete his or her own assignment. It is okay to work with other students and to ask questions in order to get ideas on how to solve the problems or how to overcome some obstacle (be it a question of Verilog syntax, how a part of the problem might be solved, etc.) It is also acceptable to seek out digital design resources for help on Verilog, digital design, the IEEE 754 floating-point format, etc. It is okay to make use of AI LLM tools such as Claude and Copilot to help understand the problems, related concepts, and solution approaches. (Do not assume LLM output is correct. Treat LLM output the same way one might treat legal advice given by a lawyer character in a movie: it may sound impressive, but it can range from sage advice to utter nonsense.)

After availing oneself to these resources **each student is expected to be able to complete the assignment alone**. Test questions will be based on homework questions and **the assumed time needed to complete the question will be for a student who had solved—not memorized the solution of—the homework assignment on which it was based**.

**Problem 1:** Solve 2025 Final Exam Problem 3, which asks for the inferred hardware of a sequential module that keeps track of trends (whether increasing then decreasing or decreasing then increasing).

**Problem 2:** Solve 2025 Final Exam Problem 4, which asks about several variations on pipelined hardware based on module `best_rot_pipe` assigned as a 2025 Homework assignment.

**Problem 3:** Solve 2025 Final Exam Problem 5, in which synthesis data on yet more variations of a `best_rot` module must be interpreted. Note that one does not need to understand what `best_rot` and friends compute to solve Problem 5, just when and how often the outputs of combinational, sequential, and pipelined modules carry results.