LSU EE 4755 Homework 6 Due: 1 December 2023

This assignment will be collected and graded, but the grades will not count.

Problem 1: Solve 2022 Final Exam Problem 1. In part a, a timing analysis is to be performed on a combinational vector normalization module `norm_comb`, and in part b a pipelined version of the module is to be designed.

Problem 2: Solve 2022 Final Exam Problem 2, in which Verilog code describing a vector normalization module, `norm_comb_n`, is to be completed.

Problem 3: Solve 2022 Final Exam Problem 3, in which a cost and timing analysis is to be done for an illustration of hardware for the `add_accum` module from 2019 Homework 6.