Final Exam Review

When / Where

Friday, 9 December 2022 15:00 (3 PM) CST

Conditions

Closed Book, Closed Notes

Bring one sheet of notes (both sides), 216 mm × 280 mm.

No use of communication devices.

Format

Several problems, short-answer questions.

Resources

Lecture "slides" and code used in class: `https://www.ece.lsu.edu/koppel/v/ln.html`

Problem Sets

Synthesis: `https://www.ece.lsu.edu/koppel/v/guides/pset-syn-seq-main.pdf`

Solved tests and homework:. `https://www.ece.lsu.edu/koppel/v/prev.html`

It is important that homework solutions be studied.

Study Recommendations

Study this semester's homework assignments **and solutions**. Similar problems will appear on the exam.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for brief hints and to check your own solutions.

Previous Exams

Be sure to look at previous midterm and final exams, but note any differences in coverage.

Course Material Areas

Verilog

The System Verilog language, including structural and behavioral code.

Synthesis

How hardware is inferred, mapped, and optimized from Verilog.

Digital Design

The functioning of the circuits covered in class.

How to design digital circuits.

How to compute cost and delay using the simple model.

Sequential Circuit Design

Pipelined Circuit Design

Tools

Understand what simulation and synthesis tools do.

Specific Circuits

Combinational and Sequential Left Shifters

Pipelined add-accumulate. (`add_accum`)

Understand the timing issues from 2019 Homework 6 module.

Multipliers

Understand the recursive constructions.

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Verilog Topics

Objects

See `https://www.ece.lsu.edu/v/2022/l020-types.v.html`.

Object Kinds: *variable* v. *net* kind of objects.

Key difference:. . .
. . . variables are assigned, nets are driven (connected to something).

Data Types

Four-State Integer Types

Two-State Integer Types

Floating-Point Types

String Type

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Integer Data Types

Four-State Integer Types: `logic`, `integer`, `time`.

Two-State Integer Types: `int`, `bit`, `byte`, `shortint`, `longint`.

Integer qualifiers: `signed`, `unsigned`.

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Real Data Types

Real Types: `real`, `shortreal`.

Reïnterpretation: `$realtobits`, `$bitstoreal`, etc..

Arrays

Packed v. Unpacked Arrays

```
uwire [7:0] e_pluribus_unum;    // Packed
uwire plain_array [7:0];        // Unpacked
```

Element and bit numbering:

```
uwire [7:0] color;    // Bit 0 is LSB.
uwire [0:7] colour;   // Bit 0 is MSB.
```

Static, Dynamic, and Associative arrays.

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Modules

Port and parameter declaration.

Module and primitive instantiation.

Object declarations.

Continuous `assign`.

Procedural code.

Generate statements.

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Object Kinds

`var` kind. (The default for `logic`, `int`, etc.)

Net kinds: `uwire`, `wire`, and other stuff we don't use in class.

Parameters

Part of module declaration: `#( int w=16, int size=10 )`.

Old-School Declaration: `parameter int w=16, size=10;`.

`localparam`.

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Procedural Code

Where procedural code can be placed.

Execution of `initial`, `always`, `always_comb`, and `always_ff`.

Delays (*e.g.*, `#5`).

Event controls (*e.g.*, `@( posedge clk )`).

Blocking v. non-blocking assignment.

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Elaboration and Generate Statements

`https://www.ece.lsu.edu/v/2022/l025-gen-elab.v.html`

Where generate statements can be placed.

Elaboration-time constants.

Describing hardware using iteration. (*E.g.*, `ripple_w`)

Describing hardware using recursion. (*E.g.*, `min_t`)

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Emphases, Key Skills

Verilog—Key Skills

Given a design in one form, write design in another:

- Explicit Structural
- Implicit Structural
- Synthesizable Behavioral
- Logic Diagram

Use generate statements to interconnect modules.

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Synthesis Key Skills

Given Verilog code:

Show inferred hardware (before optimization).

Show expected optimizations.

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Logic Design Skills

Cost and Delay Computation

`https://www.ece.lsu.edu/v/2022/lsli-simple-model.pdf`

Compute Cost using Simple Model

Compute Delay using Simple Model

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Sequential Logic Topics

Registers

Write Verilog needed to specify a register.

Determine what registers will be inferred for some Verilog.

Timing

Show a timing diagram for sequential code.

Understand timing of examples given in class:

Counters from slides: `count_thd`, etc.

Multipliers: `mult_linear_clk`, `mult_seq`.

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Synthesis Topics

Understand what is done during inference, optimization, technology mapping.
`https://www.ece.lsu.edu/v/2022/l014-syn-general.v.html`.

Inference of combinational logic.
`https://www.ece.lsu.edu/v/2022/l015-syn-comb-str.v.html`.
`https://www.ece.lsu.edu/v/2022/l045-syn-comb-behav.v.html`

Inference of registers.
`https://www.ece.lsu.edu/v/2022/lsli-syn-seq.pdf`

Optimization of combinational logic.

Use of timing constraints in synthesis.

Digital Design Topics

Common Components

- Multiplexor
- Binary Full Adder, Ripple Adder
- Integer Equality and Magnitude Comparison

Common Component Skills

- Show how to implement using basic gates.
- Know how to optimize for special cases (a constant input, etc.).

Cost and Delay Estimation

Simple Cost Model

`https://www.ece.lsu.edu/v/2022/lsli-simple-model.pdf`

Cost of n-input AND and OR gates are $(n-1)\,\mathrm{u_c}$.

Inverters (NOT gates) are free!

Delay of n-input gate is $\lceil \lg n \rceil\,\mathrm{u_t}$.

Cost of a 1-bit edge-triggered register is $7\,\mathrm{u_c}$ ...
... and delay is $6\,\mathrm{u_c}$.

Critical path **does not** pass through registers.

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Tools

Synthesis (Genus Synthesis).

- `read_hdl`, `elaborate`
- `define_clock`
- `syn_gen`
- `syn_map`
- `syn_opt`
- `report area`, `timing`

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