EE 4755—Digital Design using Hardware Description Languages

Where/When/Web

Room 201 Tureaud Hall
Mon Wed Fri 11:30–12:20 Fall 2021
`https://www.ece.lsu.edu/koppel/v/`

Who

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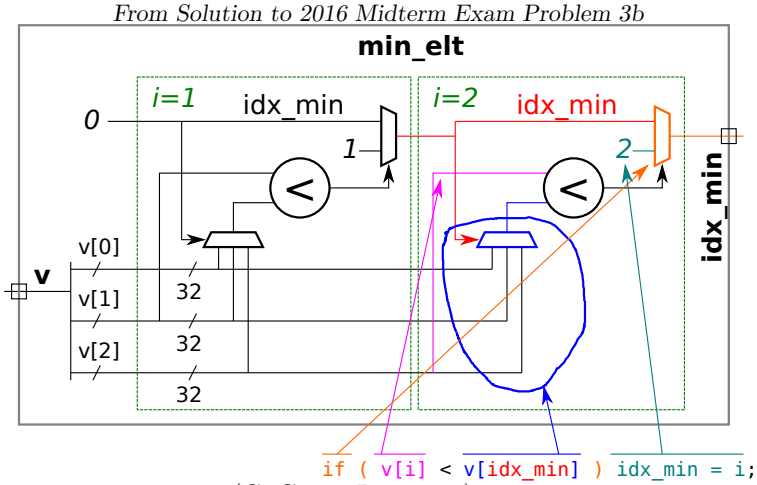
From Solution to 2016 Midterm Exam Problem 3b



Prerequisites

By Course: EE 3755.
By Topic: Logic design, computer organization, programming (C, C++, Java, etc.).

Topics

- Electronic Design Automation Big Picture: from *simulation* to get it right, to *synthesis* to make it real, and the myriad other tools between to make it good.
- SystemVerilog: data types, object types, module instantiation, procedural code, event queue and simulation timing, testbench coding.
- Synthesis Tool Usage: Design targets, timing and area constraints, design tuning, scripting.
- Inference of hardware by synthesis programs for structural and behavioral code.
- Combinational Logic Descriptions: linear and recursive structures.
- Sequential Logic Descriptions: counter-like, pipelined, state-machine controlled, etc.
- Software: Cadence Xcelium Simulator (SystemVerilog simulation), Cadence Genus Synthesis (SystemVerilog Synthesis), TCL (tool scripting).

Texts *IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language, IEEE 1800-2017.* (For a free copy visit `https://ieeexplore.ieee.org/document/8299595/`.) For those who need to review digital logic and basic Verilog: Brown & Vranesic, "Fundamentals of Digital Logic with Verilog Design" (The text used in EE 2741 and 2742.)

A.D.A.

Louisiana State University is committed to providing reasonable accommodations for all persons with disabilities. This syllabus is available in alternate formats upon request. Any student with a documented disability needing academic adjustments is requested to speak with Disability Services and the instructor, as early in the semester as possible. All discussions will remain confidential. Please contact Disability Services in 115 Johnston Hall, 225-578-5919 or at `https://www.lsu.edu/disability`.

Grading Homework assignments, including HDL coding assignments, 30%; Midterm Exam, 35%; Final Exam, 35%. Midterm exam grade may be replaced with final exam grade if that improves average. Plus/minus grading will be used. Late-homework penalty: 10% per day late deducted. Missed-midterm-exam policy: at instructor's discretion either a makeup exam, use final exam grade for midterm grade (*i.e.*, 70% final exam weight), or use zero for midterm grade. Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class whether in person or held remotely.