LSU LSU EE 4755 Homework 1 Due: 15 September 2014

Follow the instructions for class account setup and Verilog Homework Workflow, which can be found on `http://www.ece.lsu.edu/koppel/v/proc.html`*. Run the simulator code on the unmodified assignment. The output should show errors for two modules.*

Problem 1: Module `shift_right1` is supposed to perform a logical right shift on a 16-bit quantity, but it is not working properly, perhaps because the designer left for a vacation before finishing it and returned thinking that he or she had already finished it. Fix the problem.

Module `shift_right1` is written in a behavioral style, and in a way which is not synthesizable. For this problem, **do not** try to make the code synthesiable, just get the module to perform the shift properly so that the testbench does not report an error. (The module for the next problem is synthesizable.)

Your solution should assign `shifted` one bit at a time, as does the existing code. (In other words, don't just use the right shift operator.) The testbench output might provide clues to what the problem is. *Hint: The problem can be fixed with one or two lines of code.*

Problem 2: Module `shift_right2` is also supposed to perform a logical right shift. It's not working either, because it hasn't been finished. When finished `shift_right2` will make use of four `shift_right_fixed` modules. A `shift_right_fixed` module can shift by two possible amounts, zero bits (which of course is no shift at all) or `fsamt` bits, where `fsamt` is the value of a parameter.

The `shift_right2` module so far has instantiated one `shift_right_fixed` module and set the parameter to 8 (the `#(8)` indicates that the parameter is set to 8). The `shift_right2` module should instantiate three more `shift_right_fixed` modules, one each for shifts of 4, 2, and 1 bit. Instantiate the modules and connect them together so that `shift_right2` works correctly.

Hint: A correct answer will require no additional logic (beyond the three additional shifters) only declarations.