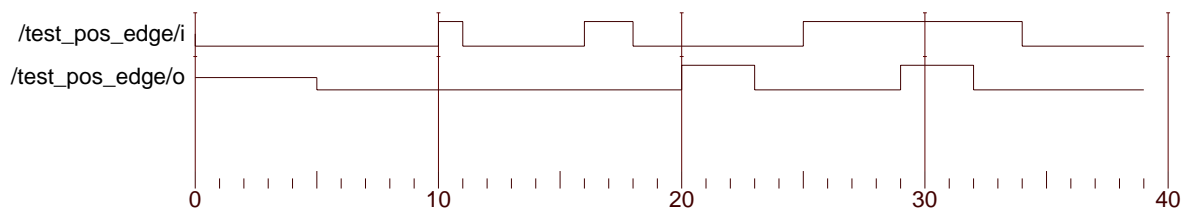


Solve this problem by modifying a copy of <http://www.ee.lsu.edu/v/2000/hw01.v>. Use Lesson 7 of the ModelSim tutorial for instructions on using the simulator as described in the references web page, <http://www.ee.lsu.edu/v/ref.html>. Instructions for submitting a solution will be given later.

Problem 1: Write two Verilog descriptions of the following circuit. The circuit has a four-bit input on which integers will appear. If the integer is equal to 2 or 9 the output should be 1, otherwise the output should be zero. One description, in a module named `number_detect_es`, should be explicit structural, and the other should be implicit structural in a module named `number_detect_is`.

Problem 2: Write a testbench for the descriptions above. Test all possible inputs. Name the testbench module `test_number_detect`.

Problem 3: The structural module below, when finished, is to produce a pulse of duration 3 ns on output `o` starting 4 ns after a positive edge on input `i`, but only if `i` is 1 for at least 2 ns. (The finished module will remain structural.) Correct operation is shown in the sample timing below where there are three pulses on input `i`. No output pulse appears at 14 ns because the input is 1 for only 1 ns. Pulses on `o` are produced for the next two positive edges on `i`. The testbench code used to generate the waveforms is in module `test_pos_edge`, already written.



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```
module pos_edge_trigger(o,i);
  input i;
  output o;
  wire noti;
  wire preout;

  assign o = preout;

  not (noti,i);
  and (preout,i,noti);

endmodule // pos_edge_trigger
```

Add delay specifications so that the module works as described. Add **only** delay specifications, nothing else. Don't add gates, don't add modules, and especially don't add behavioral code.