Multithreading

04-1

Outline

- Introduction: Types of Multithreading.

  OS-Level (not covered) v. Zero-Cycle (below) Multithreading.

- Simultaneous Multithreading

  Efficient execution of conventional multithreaded program.

  Research project, results based on simulation.

- Tera MTA

  Cacheless: threads hide memory latency.

  Thread synchronization through *presence bits* in memory.

  Commercial product in early stages of production.

References

Simultaneous Multithreading (SMT).

Description of SMT. Analysis of how variations in fetch and thread scheduling mechanisms affect performance. Simulations use multiprocessing workload (each thread from a different program).

Tullsen 96: Dean M. Tullsen, Susan J. Eggers, Joel S. Emer, Henry M. Levy, Jack L. Lo, and Rebecca L. Stamm, "Exploiting choice: instruction fetch and issue on an implementable simultaneous multithreading processor," in *Proceedings of the International Symposium on Computer Architecture,* May 1996, pp. 191–202.

Comparison of SMT with a single-chip multiprocessor having roughly equivalent total resources. Looks at resource use inefficiency in multiprocessor and impact of SMT on memory system, and other effects. Simulations use parallel workload (threads all part of one program).

Lo 97: Jack L. Lo, Susan J. Eggers, Joel S. Emer, Henry M. Levy, Rebecca L. Stamm, and Dean M. Tullsen, "Converting thread-level parallelism to instruction-level parallelism via simultaneous multithreading," *ACM Transactions on Computer Systems,* vol. 15, no. 3, pp. 322-354, August 1997.

Tera

Description of the Tera multithreaded processor.

Alverson 90: Robert Alverson, David Callahan, Daniel Cummings, Brian Koblenz, Allan Porterfield, and Burton Smith, "The Tera computer system," in *Proceedings of the International Conference on Supercomputing,* June 1990, pp. 1–6.

Short Tera program example and description of system software.

Alverson 97: Gail Alverson, Preston Briggs, Susan Coatney, Simon Kahan, and Richard Korry, "Tera hardware-software cooperation," Supercomputing 97, November 1997.

Additional information at `http://www.tera.com`.