Electrical & Computer Engineering

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Reconfigurable, low power, and ultra-stable hardware: A paradigm shift in IoT, cloud computing, autonomous sensing, and neuromorphic computations

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Abstract—The Fourth Industrial Revolution (4IR) which trending towards automation while converging digital, physical, and biological worlds through Cyber Physical System (CPS), EDGE-AI computation, Internet of Things/Everythings (IoTs/IoEs), cloud computing, 5G/6G communication, and collective artificial intelligence (AI). As an essential generic platform of such revolution, the pervasive IoT/IoE is driving the need for fundamental innovations in myriad of applications such as sensing, ubiquitous computing that enable scalable, miniaturized, secure, low power mobile and wearable devices and/or networks. However, due to unstoppable demand of data throughput and improving efficiency of the heavily connected network (trillions of devices will be interconnected i.e., the so-called TerraSwarm) that requiring miniaturized, modular, ultra-low power, autonomous, & secured transceivers or other modules that are very impractical to implement with conventional hardware. In order to overcome such aforementioned barriers, a paradigm shift in hardware development is essential in terms of power, performance & area (PPA). Therefore, this presentation will specifically focus on the development of CloudOscillator based on MEMS-referenced ultra-stable local oscillator (LO) for reconfigurable IoT transceivers, then an application of this LO will be discussed for AI-driven low power cognitive radios (CRs). More specifically, the first part of the talk will explain design, simulation, optimization, tape out, assembly, and post-Si verification of digitally-programmable & fine-grained CMOS based novel ASICs to build LO as system-on-chip (SoC) while implementing various techniques to improve its performance such as autonomous tracking the maximum stability point (stability limit to 0.5 ppm, FoM=182 dB), locked to GPS steering signal for augmenting long-term stability, multi-phase coupled oscillator arrays for digital computation, & arrays of parallel oscillators for increasing power handling capability to reduce noise. Following that, an emerging trend of these LOs in HW/SW based co-designing of multi-scale neuromorphic learning machines (comprising of heterogeneous computing resources such as ASICs, a reconfigurable processor e.g. FPGA, and a conventional CPU/GPU platform), in a hierarchical architecture to facilitating energy-efficient classification tasks will be presented. After that, a low power embedded machine learning (ML) algorithm based AI-driven reconfigurable hardware platform will be discussed towards developing next generation wireless networks to achieve higher data rates and channel capacity.

In the second part of the talk, I will present a low cost, custom-built, and short range communication platform for widespread deployment of IoT while integrating a highly sensitive and multi-sensor wireless networks (WSNs) to noninvasively monitor of human physiological signals. Additionally, I will also talk on decoding and encoding of human movement activities recorded using a Deep Brain Stimulator (DBS) sensor and using innovative neural network (NN) based ensemble classifier towards developing AI-driven & intelligent DBS system for future Brain-Machine-Brain-Interfaces (BMBI). Finally, I will conclude my talk by presenting vision towards paradigm shift in low power hardware for the IoT applications and neuromorphic system.

Bio—Mohammad S. Islam has completed his Ph. D. degree from the department of Electrical, Computer, and Systems Engineering (ECSE) at Case Western Reserve University (CWRU) in 2020, where he was working as a Graduate Research and Teaching Assistant. Prior to CWRU, He also received his MS degree in Electrical Engineering (EE) from the department of Electrical and Computer Engineering (ECE) at Florida International University (FIU). Currently, he is working as Engineer in TD at Intel Corporation. In 2020, he was working in Globalfoundries Inc., NY as a Senior Engineer Design Enablement where he was characterizing low power FINFETs from various advanced technology nodes for developing high performance FPGAs, 5G chipset, automotive, CPUs, MPUs, GPUs, and smart devices for data centers. In 2007, he was working as a Commissioning Engineer at Alcatel-Lucent in the SDH transmission department and from 2008-2012, he was working as a Senior Commissioning Engineer in ThyssenKrupp Xervon. Due to his outstanding research abilities and graduate study performance, International Student Services (ISS) at CWRU has awarded him the Elise Lindsay International Graduate Student Award in 2019. This award (the only one is awarded university-wide per year) is honored to a student who has exemplified talent, perseverance, courage, and a desire to make the world a better place. In addition, due to excellent performance in classroom teaching, he was awarded with the Outstanding Graduate Teaching Assistant (GTA) award in Spring 2015 from the department of ECE at FIU. In 2020, His paper on Global Positioning System (GPS)- disciplined MEMS-referenced oscillator was selected as the best student paper finalist award at IEEE IFCS-ISAF 2020. Aside from teaching and research, he has achieved substantial industrial experience from several multinational companies. He has received two employee spotlight awards from GlobalFoundries Inc. & many recognitions from various divisions at Intel Corporation for his excellent teamwork and collaboration efforts on multiple critical projects. He has published over 25 papers in peer-reviewed international journals and conferences, one book chapter, and has been awarded one IP. He is an IEEE member and has been served as a reviewer frequently for several reputed journals, such as IEEE TCAS-I/II, IEEE TBME, IEEE-IOT Journal, IEEE Sensors Journal. His research interests are in the areas of MEMS/NEMS based reconfigurable oscillators for RF & low power IoT applications, energy-efficient mixed signal IC (MSIC) design for analog and digital computation, chip scale neuromorphic computing, machine learning based classification tasks, AI-empowered multi-standard wireless networks, VLSI design, & emerging semiconductor device design and fabrication.

When: Friday, **29 April 2022,** 11:45 - 12:45
Where: Room 3250H Patrick F. Taylor Hall
Info: https://www.lsu.edu/eng/ece/seminar