## Electrical & Computer Engineering $\begin{array}{c} \textbf{S} \hspace{0.1cm} \textbf{E} \hspace{0.1cm} \textbf{M} \hspace{0.1cm} \textbf{I} \hspace{0.1cm} \textbf{N} \hspace{0.1cm} \textbf{A} \hspace{0.1cm} \textbf{R} \\ \textbf{Louisiana State University} \end{array}$

## Physical and Electrical Properties of Hot Carrier Degradation of Si MOS Transistors Processed in D<sub>2</sub> and H<sub>2</sub>

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Abstract—Extensive experimental investigation has been carried out to study the hot carrier life time improvement due to deuterium annealing of MOS transistors with one level and multi-levels of metalization. 10-80 times improvement has been demonstrated in both one level and multi-levels of metalization. The demonstration of large life time improvement of transistors with multi-levels of metalization leads to the development of using deuterium annealing in the manufacture of integrated circuits at Lucent Technologies.

The classical concept suggests that degradation of MOS transistors is caused by interface trap generation resulting from "hot carrier injection". In order to understand the mechanism of interface trap generation, the MOS transistors have been subjected to various carrier injections into the oxide such as anode hole injection and substrate hot electron injection. These experiments show clearly that hot carrier injection into the gate oxide exhibits essentially no isotope effect, whereas, channel hot electrons at the interface exhibit a large isotope effect. This leads to the conclusion that channel hot electrons, not carriers injected into the gate oxide, are primarily responsible for interface trap generation for standard hot carrier stressing. In addition, a simple model has been proposed to explain the saturation of the transconductance degradation.

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