MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

AUTOMATIC CONTROL TOPICS

A. Basic Tools
Laplace, Z transforms: basic properties, use in solving linear differential/difference equations, application to system analysis, transfer functions. Fourier transform, Fourier series: basic properties, application to signal analysis, frequency response, spectral energy density.

B. Basic Concepts
Linearity, time invariance, causality, difference and differential systems, linearization, signal-flow and block diagrams, BIBO and asymptotic stability.

C. Classical Control
Transient and steady state analysis and performance indicators, pole location, sensitivity; frequency domain analysis, phase and gain margins; Nyquist stability, Routh-Hourwitz criterion, root locus, lead and lag compensator design, PID control; pole placement with fractional controllers.

D. Sampled Data Systems
Basic A/D and D/A conversion, sampling theorem. Discretization of continuous time systems, deadbeat control.

E. State Space Control for Continuous and Discrete Time Systems
State and state equations, transition matrix, solution of state equation. Realization, controllability and stabilizability, observability and detectability, Lyapunov stability, state feedback and pole placement, asymptotic observers, state feedback with observers.

Representative References

1.   C-T. Chen, *System and Signal Analysis*, Saunders College Publishing.
2.   B.C. Kuo, *Automatic Control Systems*, Prentice Hall.
3.   G.F. Franklin, J.D. Powell, A. Emami-Naeini, *Feedback Control of Linear Systems*, Addison Wesley.
4.   G.F. Franklin, J.D. Powell, M.L. Workman, *Digital Control of Dynamic Systems*, Addison Wesley.
5.   K. Ogata, *Discrete-time Control Systems*, Prentice Hall.
6.   W.L. Brogan, *Modern Control Theory*, Quantum Publishers, Inc.
7.   T. Kailath, *Linear Systems*, Prentice Hall.
8.   K. Ogata, *Modern Control Engineering*, Prentice Hall.
9.   C. T. Chen, *Linear system Theory and Design*, 3rd Ed., Oxford University Press, 1999.

M.S. Comprehensive /Ph.D. Qualifying Exam
Communication and Signal Processing Topics

Probability Theory and Random Processes
Basic concepts in probability theory; stationarity and wide sense stationarity of random processes, power spectral density, linear filtering of random processes, minimum mean squared error estimation, Gaussian and Poisson random processes.

Signals, Systems, and Digital Signal Processing
Continuous time and discrete time signals and systems: fundamental concepts, system properties (causality, stability, time invariance, etc.); time and frequency domain characterization of discrete and continuous time signals and systems; transform domain techniques; sampling and reconstruction; sampling rate conversion, frequency-domain analysis, aliasing and Nyquist rate concepts; discrete Fourier Transform and FFT algorithms; design and implementation of FIR and IIR filters.

Analog Communication
Amplitude modulation techniques; frequency and phase modulation techniques; sampling, quantization; pulse code modulation (PCM); effect of noise on continuous wave and PCM systems.

Digital Communication
Signal space representation; baseband representation of bandpass signals and systems; maximum likelihood (ML) detection and estimation; optimum receiver principles. performance of optimum receivers; differential, partially coherent and non-coherent detection of signals; bandwidth efficiency and power efficiency; receiver design and performance analysis of digital modulation schemes in fading channels; linear block codes and their decoding strategies, hard decision and soft decision decoding.

Representative References

1. Simon Haykin, *Communications Systems*, (Wiley).
2. J. G. Proakis and M. Salehi, *Communication Systems Engineering, 2nd Edition*, Prentice Hall.
3. J. G. Proakis, *Digital Communication*, 4th Edition, McGraw-Hill, 2000.
4. J. M. Wopzencraft and I. M. Jacobs, *Principles of Communication Engineering*, John Wiley & Sons, New York, 1965.
5. Henry Stark and John W. Woods, *Probability and Random Processes with Applications to Signal Processing, 3rd Edition.* Prentice-Hall.
6. *Probability, Random Variables, and Stochastic Processes*, A. Papoulis, 3rd edition, McGraw-Hill, 1991.
7. S. K. Mitra, *Digital Signal Processing*, 3rd edition, McGraw-Hill.
8. A. V. Oppenheim and R.W. Schafer, *Discrete-time Signal Processing*, Prentice-Hall.

MS COMPREHENSIVE / PHD QUALIFYING EXAM

COMPUTER ENGINEERING TOPICS

Appearing below is an outline of topics which computer-area questions will be based on. Most of the topics clearly fall into one of the three question areas, Hardware, Software, and Applications, but questions in one area can draw on topics from other areas. For example, the solution to an algorithm (software) question might require knowledge of cache organization (hardware).

Topics described with "Proficiency in" (or similar wording) must be understood very well, as though you were going to take a test in a course covering the topic. Topics described using "Competence with" (or similar wording) must be understood well enough to solve problems or answer substantive questions, however definitions or other background might be provided as part of the question. This information should help students that know the material make a quick start solving the problem. For topics listed under "Familiarity with" students should have a basic background in the area, including basic terminology, but need not know many specifics. For these problems a greater amount of background will be provided, enough so that a good student might be able to solve them without having taken any courses covering the topic.

Logic Design
Proficiency with combinational and sequential logic theory at EE 2720 and EE 2730 level, including Boolean algebra and basic minimization techniques. Proficiency in designing basic combinational and sequential circuits.

Computer Arithmetic
Proficiency with signed integer representations and with full adder and carry look-ahead adder designs. Competence with basic integer multiplication and division circuits. Competence with floating-point (FP) representations, including IEEE 754, and with FP arithmetic. Familiarity with modular and residue arithmetic.

Computer Instruction-Set Architecture (ISA) and Microarchitecture
Proficiency with 5-staged pipelined RISC (e.g., MIPS) implementations, including design rationale, direct and bypassed data paths, control signals, and relationship between implementation and instructions. Competence in assembly language programming, including RISC instruction sets. Competence with instruction set design issues, including memory addressing modes, and the variety of jumps & branch instructions. Familiarity with interrupts, traps, and exceptions. Familiarity with pipeline depth and superscalar width issues. Familiarity with caches and branch prediction techniques.

Computer Communication Networks
Competence with basic switching and multiplexing techniques. Familiarity with network layers and protocol stacks, ARQ protocols, error detection and correction. Familiarity with Internet addressing and routing standards and techniques. Familiarity with network reliability, availability, structural reliability terminology and techniques.

Algorithms and Data Structures

 Proficiency with basic data structures (including arrays, stacks, linked lists, trees), basic algorithms (including binary search, merge sort, tree searches), memory content and layout of numbers, pointers, arrays, and structures complexity analysis of algorithms. Competence with advanced data structures (including hash tables, graph representations), algorithmic paradigms (including divide and-conquer, greedy, dynamic programming) and analysis techniques (including recurrence relations, amortized analysis). Familiarity with computational complexity and intractability randomized, online and approximation algorithms.

Parallel and Distributed Computing

Competence in major parallel system organization topics including hardware organizations (CPU & network), parallel program organizations (processes, tasks, or threads), communication models (message passing or shared memory). Competence with metrics for analysis of performance including speedup, efficiency, time complexity, and space complexity. Competence with use and implementation of basic synchronization primitives and constructs including compare & swap, atomic memory operations, semaphores, and barriers. Competence with basic parallel algorithms including reduction, sorting, leader election, graph algs, etc. Competence with common interconnects including bus, crossbar, mesh, hypercube networks.
Familiarity with other interconnects including Log n stage networks (e.g., omega), Clos and Benes networks.

Operating Systems and Compilers

Competence with coordination concepts, constructs, and issues, including multiple-process access to shared structures, mutual exclusion, and deadlock. (See also basic synchronization topics under Parallel and distributed computing.) Competence with basic memory management issues including virtual and physical addresses and their rationale virtual to physical address translation techniques, page swapping basics. Competence with program compilation techniques, including control-flow and data-flow program representations, dependencies and dependence testing, common optimizations, and common program transformations.

Computer Vision and Image Processing

Proficiency in geometric and radiometric image formation. Proficiency in image segmentation, enhancement and restoration techniques. Competence in image compression and morphological image processing. Familiarity with pattern recognition techniques.

Logic Testing and Reliability

Familiarity with fault models, including the stuck-at model.

MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

ELECTRONICS ENGINEERING TOPICS

A. Circuits

Circuit applications of diodes. Circuit applications of BJT, MOSFETs and JFETs in linear and digital circuits. Linear applications include amplifiers, oscillators, differential amplifiers and operational amplifiers. Applications of ideal operational amplifiers. Digital applications include internal operation of standard logic gates used as building blocks in logic families such as TTL, ECL, NMOS and CMOS.

B. Devices

Basics of carrier transport in semiconductor materials, physics of p-n junction diodes, bipolar and field effect transistors. Derivation of terminal current-voltage characteristics of discrete devices, large and small signal models. Basic physics of photonic devices. Basic integrated circuit technology.

C. Fields

Static fields, Maxwell's equations, propagation through istropic medium, reflections and basic antenna theory.

Representative References

1. M.N. Horenstein, *Microelectronic Circuit and Devices*, Prentice Hall.
2. Mitchell & Mitchell, *Introduction to Electronic Design*, 2nd Ed., Prentice Hall.
3. Gray & Mayer, *Analysis and Design of Analog Integrated Circuits*, 3rd Ed., John Wiley.
4. D. A. Hodges, H. G. Jackson and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, 3rd Ed., McGraw-Hill.
5. B. Streetman, *Solid State Electronic Devices*, 3rd Ed., Prentice Hall.
6. J.P. McKelvey, *Solid State and Semiconductor Physics*, Harper & Row.
7. Shen, *Applied Electromagnetics*, 2nd Ed., Prindle-Weber-Schmidt.

COMPREHENSIVE MS/QUALIFYING PH.D. EXAM

POWER ENGINEERING TOPICS

A. Electric Machinery
    Maxwell's equations; analysis of simple electromechanical devices using Maxwell's equations; synchronous machines, voltage behind reactance model, Park transformation, d,q equations; exact and approximate equivalent circuits of single-phase transformers, nonlinear effects; modeling and calculation of its parameters of transmission lines; modeling and analysis of direct current and induction machines.

B. Power Systems
    Per-unit calculations; symmetrical components; sequence impedances of transformers, synchronous machines and induction motors, sequence impedances and capacitances of transmission lines; sequence networks for fault analysis; shunt faults (3-phase, LG, LLG, LL faults); series faults (1LO, 2LO); power flow equations, (Decoupled) Newton-Raphson, Gauss/Gauss-Seidel methods; optimal dispatch with/without line losses; transient stability, swing equation, equal area criterion, effect of clearing time; low-frequency oscillations, supplementary excitation/governor control; linear optimal stabilization.

C. Power Electronics
    Fourier series of nonsinusoidal voltages and currents; analysis of circuits with nonsinusoidal voltage and current waveforms, nonsinusoidal active and apparent powers; single-phase and three-phase rectifiers, controlled AC/DC converters, DC/DC converters, inverters.

Representative References

1. R.D. Schultz & R.A. Smith, *Introduction to Electric Power Engineering,* John Wiley, 1988.
2. V. DelToro, *Electric Power Systems*, Prentice Hall, 1992.
3. P.M. Andersen, *Analysis of Faulted Power Systems*, The Iowa State Univ. Press, 1983.
4. Y.N. Yu, *Electric Power System Dynamics*, Academic Press, 1983.
5. M.H. Rashid, *Power Electronics*, Prentice Hall, 1988.
6. N. Mohan, T.M. Undeland, W.P. Robbins, *Power Electronics*, John Wiley, 1989.

Because they represent unsigned integers in binary, conventional processors can quickly perform operations like $r2^i$ and $\lfloor r2^{-i} \rfloor$, where r is the contents of a register and i is a small value. Suppose it were necessary to quickly perform operations such as $r3^i$ and $\lfloor r3^{-i} \rfloor$. Conventional processors would have to resort to time-consuming multiply and divide instructions. These operations could be quickly performed if the underlying integer representation was in radix 3 (ternary) rather than in radix 2 (binary). Consider a CPU that keeps integers in a binary-coded ternary (BCT) representation. The representation is stored in conventional two-state logic but each ternary digit is encoded using two bits.

(a) Design an n-ternary-digit adder for such integers (which are represented using $2n$ bits) using basic logic gates and binary full- and half-adders. The design should be in the form of a ripple adder adapted to BCT so that it takes $O(n)$ time and uses $O(n)$ hardware.

(b) Design propagate and generate circuits for the BCT adder that can be used to construct a carry lookahead BCT adder.

Let $S = \{s_1, s_2, \cdots, s_z\}$ be a set of binary strings of maximum length n. For any string s_i of length $\ell \leq n$ and any integer $1 \leq \alpha \leq \ell$, its α-prefix is the string consisting of the first α bits of s_i. If $\alpha > \ell$, then the ℓ-bit string does not have an α-prefix.

For $1 \leq \alpha \leq n$, let $k = k_1 k_2 \cdots k_\alpha$ be an α-bit binary string called the *key*. (Note that α should not be considered fixed as it could be different for different instances of the problem.) This question involves finding the longest string(s) in S whose α-prefix equals the key. In this problem we will call these string(s), the *longest string(s) of the key*. There could be 0, 1 or multiple longest strings for a given key.

Answer the following questions. All answers must be justified.

(a)   Let $S = \{0, 11, 110, 1101, 1111\}$. Find all longest string(s) of S with the following key k as prefix.

    (i) $k = 110$

    (ii) $k = 01$

    (iii) $k = 11$.

(b)   For this part assume that for any given key the longest string, if it exists, is unique. Design a hardware module to find the longest string in S for any given k.

Assume that the key is input through a $O(n)$-bit register and that the set S is stored in a bank of $O(n)$-bit registers. The output is a $O(n)$-bit longest string or an indication that no such string exists. You can also assume that the gates used in your design allow unbounded fan-in and fan-out.

Speed should be the main objective of your design. For two equally fast solutions choose one with less hardware cost. Find the order of time needed for your solution.

(c)   How would you approach the problem if there could be multiple longest strings for a given key. Assume here that the lexicographically earliest string is output in case of multiple matches.

This question is regarding to cache design.

(a) For the same cache size, is it possible for a direct-mapped cache having a better hit rate than a fully associative cache? If so, give an example for the access pattern or the program using the caches; if not, justify the reason.

(b) For the same cache with different replacement policies, is it possible for the cache with the least-recently-used (LRU) policy having a better hit rate than the optimal (OPT) replacement policy? If so, give an example for the access pattern; otherwise, explain why not?

(c) For a dual-core processor, there is a shared last level cache between the two cores. Two threads (T1 and T2) can run either individually or simultaneously. When the threads running individually, the last level cache hit ratio for the two threads (T1 and T2) are H1 and H2 respectively. When the threads running simultaneously, the last level cache hit ratio for the two threads (T1 and T2) is H1' and H2' respectively. Is it possible for H1' > H1 and H2' > H2? If yes, list an example for the access patterns or write the programs; otherwise, justify your answer.

Usually, we have two policies for memory disambiguation in an out-of-order executed processor: (1) a conservative solution is stalling a load instruction and its dependent instructions until the early store's address generation; (2) another alternative is predicting the memory dependence between loads and earlier outstanding stores. Memory dependence prediction allows loads to bypass earlier stores if no dependence is predicted. Otherwise, if dependence is predicted, load values can be forwarded from the latest earlier stores without cache access. At the commit stage of stores, the processor check correctness of predictions, if not, loads and their dependent instructions would be re-executed.

Now consider a two-issue, out-of-order execution pipeline with following stages: Instruction Fetch (IF), Decode (ID), Issue (IS), Execution / Address Generation (EX), Write Result (WR), Commit (CT). There are two integer ALU units, two load/store units and one MUL unit.

For the following code section, the EX stage for MUL instructions requires 10 cycles. All other instructions' EX stages have only 1 cycle. Please note that SW instructions only write cache in CT stage.

1. MUL	R2, R11, R12
2. SW	R1, 0(R2)
3. LW	R3, 20(R4)
4. ADD	R5, R3, R6
5. LW	R7, 100(R8)
6. SUB	R9, R7, R8
7. ADDI	R10, R5, 20

(a) If this pipeline employs the policy (1) mentioned above for memory dependence, show execution steps with timing for the above code section.

(b) If this pipeline employs the policy (2) mentioned above for memory dependence, the memory dependence predictor predicts that there is no dependence for both loads. Two loads (inst. 3 and 5) are executed without stalls. However, after the store address generation, instruction 3 has a true dependence with instruction 2 but instruction 5 doesn't have, show execution steps with timing for the above code section.

(c) Design a memory dependence predictor. The predictor would provide two predictions: dependence, no dependence. Draw a diagram for your design and specify the circumstances for each prediction.

Let $*$ be any associative binary operation. The *prefix computation* (with respect to $*$) on an array $A = \langle a_0, a_1, \cdots, a_{n-1} \rangle$ produces a second array $B = \langle b_0, b_1, \cdots, b_{n-1} \rangle$, where $b_i = a_0 * a_1 * \cdots * a_i$, for any $0 \leq i < n$. The figure below shows prefix computation circuits for $n = 4$ and 8. In these figures, each box represents hardware for applying $*$ to its two inputs.
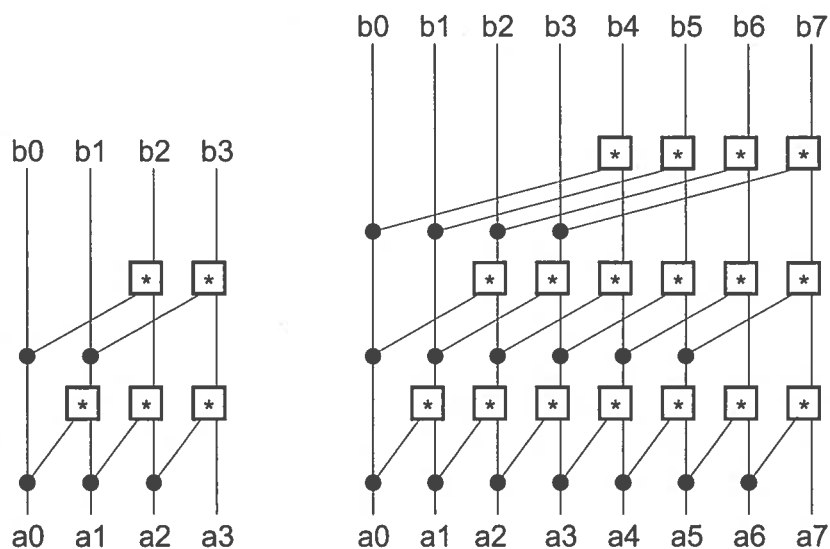

(a)   Draw a similar prefix computing circuit for 16 inputs.

(b)   Adapt the given circuit for 8 inputs to work for 5 inputs.

(c)   Describe the circuit for the general case of $n = 2^k$ inputs, and prove that it correctly performs the prefix computation.

(d)   Observe that adding 1 to an n-bit number amounts to complementing all lower order bits up to the first 0. For example, $10110\ 0111111 + 1 = \overbrace{10110}^{\text{unchanged}}\ \underbrace{1000000}_{\text{complemented}}$.

An n-bit binary counter counts up from 0 to $2^n - 1$ and then back to 0. Describe how a fast prefix computing circuit can help build a fast counter.

(a) "In the field of computer science, a binary decision diagram (**BDD**) or a propositional directed acyclic graph (PDAG) is a data structure that is used to represent a Boolean function The data structure is created using the *Shannon expansion* where a switching function is split into two sub-functions (cofactors) by assigning one variable (cf. *if-then-else normal form*). [Wikipedia]."
For example, the BDD for an AND gate with inputs x1 and x2 is as follows:
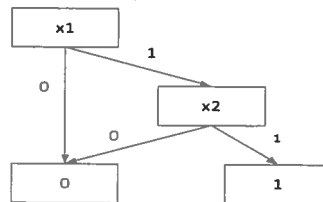
BDD for a 2-input AND gate

Using this concept, show the BDD for a (i) 2-input OR gate with inputs x1 and x2 and (ii) 1-bit Full Adder with inputs A_i, B_i, and C_{in} and outputs S_i and C_{out}.

(b) In the figure shown above (BDD for a 2-input AND gate), if each event (x_i as 1 or 0) is equally likely, find the probability of (a) output being 1 and (b) output being 0. What will happen to (b) if the probability of x_i being 1 changes to ¾ ?

In many applications a high-dimensional relationship is represented in fewer dimensions. This problem involves representing a two dimensional $N \times N$ mesh in a one dimension. Part (a) of the figure below shows a 4×4 mesh with elements numbered by two dimensional coordinates (r, c), where $0 \leq r, c < 4$ are the row and column numbers.

   (a) 2D coordinates   (b) row-major   (c) snake   (d)Z-order
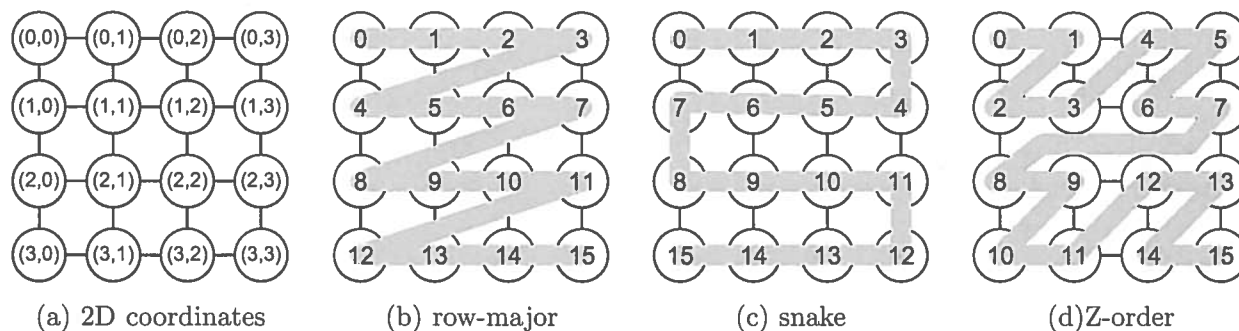
Let $\mathbb{N} = \{0, 1, \cdots, N - 1\}$. Then $\mathbb{N} \times \mathbb{N}$ is the set of all doublets in the $\mathbb{N} \times \mathbb{N}$ "plane;" part (a) of the figure above shows these doublets for $N = 4$. Let $\mathbb{S} = \{0, 1, \cdots, N^2 - 1\}$; verify that $\mathbb{N} \times \mathbb{N}$ and $\mathbb{S}$ have the same number of elements. A 1-dimensional projection (or mapping) of $\mathbb{N} \times \mathbb{N}$ is a bijection $f : \mathbb{N} \times \mathbb{N} \longrightarrow \mathbb{S}$ that maps the doublets (2-dimensional quantities) of $\mathbb{N} \times \mathbb{N}$ to unique (1-dimensional) numbers of $\mathbb{S}$. Parts (b)–(d) of the figure above show three such projections; the underlying shading traces the numbers 0 to 15 in order.

The $N \times N$ mesh has $2N(N - 1)$ edges. For any edge $e = (u, v)$, where u, v are nodes and a given 1-dimensional projection f, define the *dilation* of e (with respect to f) as $|f(u) - f(v)|$. Each edge of the mesh connects nodes that are "adjacent" in the relationship represented by the mesh. The dilation of the edge represents the distance the 1-dimensional projection has induced between the nodes u, v connected by e. The average of the dilations of all $2N(N - 1)$ edges of the mesh is the *dilation of the projection f*.

For example consider the edge between nodes $(0, 3)$ and $(1, 3)$. In the three projections shown in parts (b)–(d) above, the dilations of this edge are 4, 1, and 2, respectively.

(a)   Determine the dilations of the edge between nodes $(1, 0)$ and $(2, 0)$ in the above three projections.

(b)   For an $N \times N$ mesh, prove that the dilations of the projections shown in parts (b) and (c) of the above figure is $\Theta(N)$.

(c)   With $N = 2^n$ for some integer $n \geq 1$, prove that for an $N \times N$ mesh, the dilation of the projection in part (d) of the figure above is $O(N \log N)$.

   Hint: Observe that the projection recursive connects the four quadrants of the mesh as a "Z." Determine a recurrence relation for an upper bound on the dilation and solve it.

Let $G = (V, E)$ with n vertices and m edges be an undirected graph with weighted edges. Suppose we are given a minimum spanning tree T of G. Now let a new edge $e = (u, v)$ with weight $w(e)$ be added to G. Let $G + e$ denote the graph with added edge e.

(a) Construct an efficient algorithm to test whether T remains a minimum spanning tree of $G + e$. Note any assumptions that you make about what data structures are used to represent tree T and graph G. Analyze the time complexity of your algorithm and explain why it is correct.

(b) Suppose that T is no longer a minimum spanning tree. Construct an efficient algorithm to update tree T to a new minimum spanning tree. Analyze the time complexity of your algorithm and explain why it is correct.

Let A denote an array with n distinct elements. The INSERTION-SORT algorithm is as follows.

```
INSERTION-SORT(A)
    for j = 2 to n
        key = A[j]
        i = j - 1
        while i > 0 and A[i] > key
            A[i+1] = A[i]
            i = i - 1
        A[i+1] = key
```

(a) Define an inversion as follows: "If $i < j$ and $A[i] > A[j]$, then the pair (i, j) is called an inversion of A." For an array A, prove that INSERTION-SORT runs in time $O(n + I)$, where I is the number of inversions in A.

(b) Let A denote an array of "nearly sorted" elements, that is, each element in A is within g positions of its correct location. For a nearly sorted array A, prove that INSERTION-SORT runs in time $O(ng)$.

We want to run a multi-task application on a square mesh of cores, where the mesh has size $m \times m$, the application with $n \leq m^2$ tasks, and we can map at most one task to each core. For an application with multiple tasks, let a task graph for that application contain a vertex v_i for each task t_i and an edge (v_i, v_j) for each pair of communicating tasks t_i and t_j. Edge (v_i, v_j) has weight $w(v_i, v_j)$ equal to the number of bits communicated between tasks t_i and t_j. If core c_x handles task t_i and core c_y handles task t_j, then the communication energy for this pair of tasks is $w(v_i, v_j)$ times η (a bit-energy constant) times the Manhattan distance between c_x and c_y. (The Manhattan distance is the magnitude of the difference of the row indices plus the magnitude of the difference of the column indices.) Given a two-dimensional mesh of cores and a task graph, the *task mapping problem* is to map each task to a core (at most one task to a core) in a way that minimizes communication energy.

Describe two heuristics to approximately solve the task mapping problem. Identify the strengths and weaknesses of both. Specify which of the two heuristics you expect to perform better and explain why.

Let $G = (V, E)$ denote an undirected graph in which each edge $e_i \in E$ has bandwidth $b(e_i)$. The *bottleneck rate* $b(P)$ of a path P between two vertices u, v is the minimum bandwidth of any edge in P. The *best achievable bottleneck rate* for pair u, v is the maximum over all paths P between u and v of the value $b(P)$.

Prove that a spanning tree T exists in G such that, for every pair of vertices u, v, the bottleneck rate of unique path in T between u and v is equal to the best achievable bottleneck rate for u, v. Give an efficient algorithm to construct such a spanning tree. Derive the time complexity of your algorithm.

Consider a system in which a counter needs to be incremented using bit level operations. It is well-known that to increment a binary number, all you need to do is complement all the bits from the right up to the rightmost 0. For example incrementing 1010 1011 0111 1111 gives $\underbrace{1010\ 1011}_{\text{unchanged}}\ \underbrace{1000\ 0000}_{\text{complemented}}$. For this problem the cost of the incrementing equals the number of bits complemented.

Answer the following parts. All answers must be justified.

(a)   Determine the cost of increment the following binary numbers.

   (i)   000
   (ii)   010
   (iii)   111

(b)   What is the worst case cost of incrementing an n-bit counter?

(c)   If the n-bit counter is incremented from 0 to $2^n - 1$, then prove that the amortized cost per increment (that is, the average cost per increment) is $O(1)$ (upper bounded by a constant).

   For this part, you can use the fact that $\sum_{i=1}^{n} \frac{i}{2^i} = 2 - \frac{n+2}{2^n}$.

(d)   To prove part (c), is it necessary for the counter to start at 0?

(1) (2)
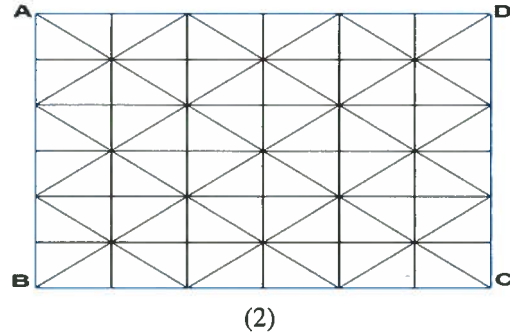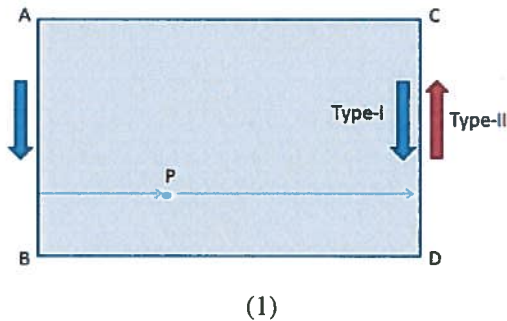
Given a rectangle patch $ABCD$ (Figure (1)). If you glue AB with CD, following the direction indicated by the Type-I arrow, you will get a *cylinder*. But if you glue AB with DC instead, i.e. A glued to D, B glued to C, following the direction indicated by Type-II arrow, you will get a *Möbius strip*. Suppose there is a 2D robot living in a giant planet that is either a *cylinder* or *Möbius strip*, can you develop algorithms to help the robot identify whether the planet is a *cylinder* or a *Möbius* strip?

(a) Suppose the robot can move freely on this surface, but it can only examine and mark a very small neighboring region on the surface to detect whether a point is on the boundary and label it when needed. Describe an algorithm for the robot to differentiate the cylinder and Möbius strip.

(b) This is another method. Suppose the robot has a way to tessellate the planet to F triangles, E edges, and V vertices, as shown in Figure (2). And the robot can mark arrows along edges inside faces, then use the consistency of the directions of arrows from neighboring faces to differentiate the cylinder and Möbius strip. Develop an algorithm based on this idea, and analyze its time complexity.

1

Given two points $v_1 = (x_1, y_1)$ and $v_2 = (x_2, y_2)$, any point p located on line segment $[v_1, v_2]$ can be represented by:

$$p = (1 - \lambda)v_1 + \lambda v_2, \tag{1}$$

where $0 \leq \lambda \leq 1$ is called p's barycentric coordinate. The barycentric coordinate for any point between v_1 and v_2 is between 0 and 1, and it is linear with respect to v_1 and v_2.

(1) Now consider three non-collinear points v_1, v_2, v_3, which forms a triangle $[v_1, v_2, v_3]$. Any point p inside triangle $[v_1, v_2, v_3]$ can also be represented using barycentric coordinates linearly that interpolates these three points. Derive the barycentric coordinates for a point inside the triangle. Note that coordinates should have each of its components ranging inside $[0, 1]$.

(2) Further generalize this barycentric coordinates to $n, (n > 3)$ points in n-dimensional space.

An image whose profile is given across an edge in Fig 1 is deteriorated with a white Gaussian noise.

  i.   Propose an operator (single operator or composition of operators) that processes the image with a kernel-based function to reduce effect of the noise and to detect the edge.
  ii.   What is the purpose of using this kernel-based function proposed; what type of a filter can it be?
  iii.   How does your operator detect the edge pixel?
  iv.   Illustrate your answers over the image profile.
  v.   How can you increase computation performance of your operator for multiple images?
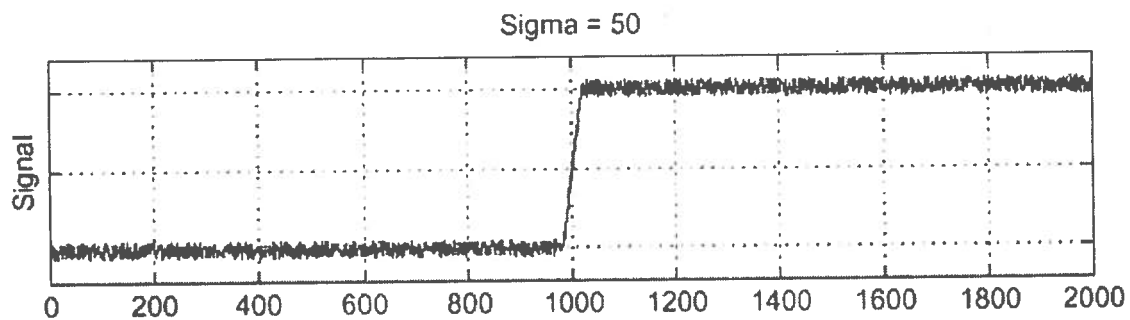
Fig 1 Image profile across an edge

Assume that an image is represented by its average image index *AvIndx* defined in equation (1). As an engineer you propose a similarity index, called normalized average image difference *NAID* defined in equation (2), between two images based on their *AvIndx*. You are asked to compare two images I_1 and I_2 whose elements are non-negative.

  a. How would you test whether this method is 'robust' to a noise in the images compared?
  b. What would be the relation between the *NAID* and a threshold *T* such that the proposed similarity measure is 'robust'? Explain your answer formally. State all assumptions you consider.

The proposed similarity measure: Two images are said to be dissimilar if their normalized average image difference *NAID* is greater than a threshold *T*. Hint: Signal = Original Signal + Noise.

$$AvIndx(I) = \frac{\sum_{x,y} I(x,y)}{N} \qquad\qquad (1)$$

$$NAID(I_1, I_2) = \frac{|AvIndx(I_1) - AvIndx(I_2)|}{\sum_{x,y} I_1(x,y) + I_2(x,y)} \qquad\qquad (2)$$

This problem involves an asynchronous distributed system of nodes connected in a ring. Each node has a unique id (that also a reflects a priority) for the problem below.

Let the nodes be $v_0, v_1, \cdots, v_{n-1}$ connected in a ring in the order shown. Let the id of v_i be x_i; note that the x_i may not be ordered on the ring. Each pair of adjacent nodes, v_i and $v_{(i+1)(\bmod n)}$, shares a resource. That is, each node has two shared resources associated with it. There is a *conflict*, if two adjacent nodes attempt to access the same resource simultaneously.

The object is for each node to access each of its two resources one time without conflict. We will require that higher id nodes have higher priority than lower id nodes.

Consider the following algorithm for the problem.

- Each node communicates its id with its neighbors in the ring

- If a node has higher priority than both its neighbors, it accesses (both of) its resources.

- It changes its priority to be $-\infty$ (very low) and informs its neighbors.

(a)   Illustrate the algorithm for two small cases, one in which it proceeds very fast and another in which it proceeds very slow.

(b)   For the general case of the n-node ring, what is the best case and worst case time complexities of the algorithm. What is the order of messages sent over the ring. Explain your answers.

(c)   Prove that the algorithm is conflict free for the general case of n nodes.

(d)   Prove that the algorithm terminates for the general case of n nodes. For this part assume that the algorithm terminates when all nodes have accessed their resources.

Given a set of points $P = \{p_1, p_2, \ldots, p_n\}$ on a line segment L. A Voronoi Diagram $V(P)$ is a decomposition of L determined by P. The Voronoi diagram $V(P)$ partitions L into n segments $V(P) = \{v_1, v_2, \ldots, v_n\}$. Each segment v_i corresponds to a point p_i, consisting all points closer to p_i than to any other points p_j:

$$v_i = \{p | p \in L, |p - p_i| < |p - p_j|, j \neq i\}.$$

(1) Given L and the point set P, design an algorithm to find the decomposition of L and analyze your algorithm's complexity.

If we further try to optimize all the points $\{p_i\}$ to minimize the following energy:

$$F(P) = F(p_1, p_2, \ldots, p_n) = \sum_{i=1}^{n} \int_{v_i} |x - p_i|^2 dx$$

(2) Explain when a minimizer of F is found, how will P distribute and why. Design an algorithm to solve this optimization.

A half-plane $h(a, b, c)$ is a region in R^2 defined as $h(a, b, c) = \{(x, y) | ax + by \leq c\}$.

Given a set of half-planes $\{h_1, h_2, \ldots, h_n\}$, defined by $\{(a_1, b_1, c_1), (a_2, b_2, c_2), \ldots, (a_n, b_n, c_n)\}$ respectively, prove that (1) the intersection of all these half-planes is a convex region; (2) this convex region is a polygonal region whose boundary has at most n straight edges.

Note that: 1) a region Ω is convex if for every pair of points within this region, $\forall p, q \in \Omega$, any point on the straight line segment that joins them is also within the region, namely, $\overline{pq} \subset \Omega$.

2) A region is a polygonal region if its boundary is formed by a set of line segments. And this region can be unbounded.

Circuits and Systems
Problem 1

In the circuit below a 0 to 5V square wave is applied to the input.

a) What is the output voltage when the input square wave is high?

b) What is the charge on the capacitor when the input square wave is high?

c) What is the charge on the capacitor when the input square wave is low?

d) How much charge is transferred from the positive supply to ground each cycle.

e) What is the current drawn by the circuit if the input square wave is at a frequency of 1 kHz?
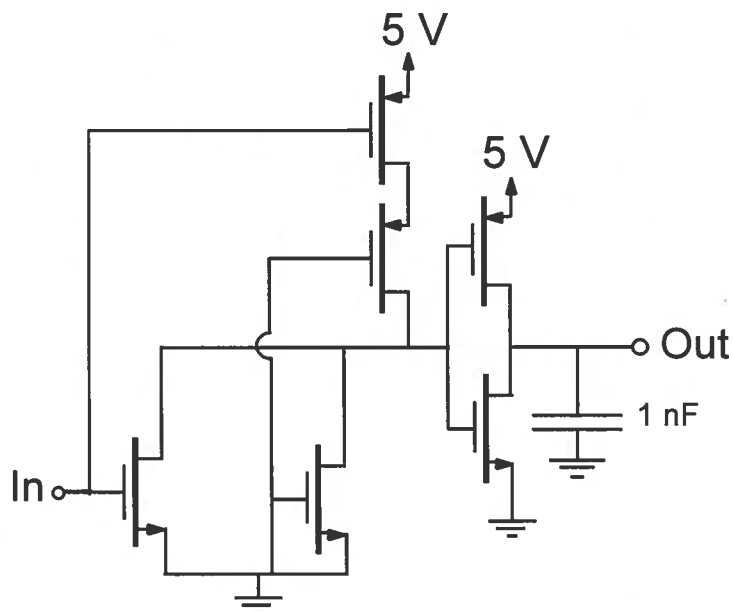
Circuits and Systems
Problem #2

a) For the CMOS inverter shown below, calculate and plot the current that flows through the transistor as a function of $0 \leq V_{IN} \leq V_{DD}$.
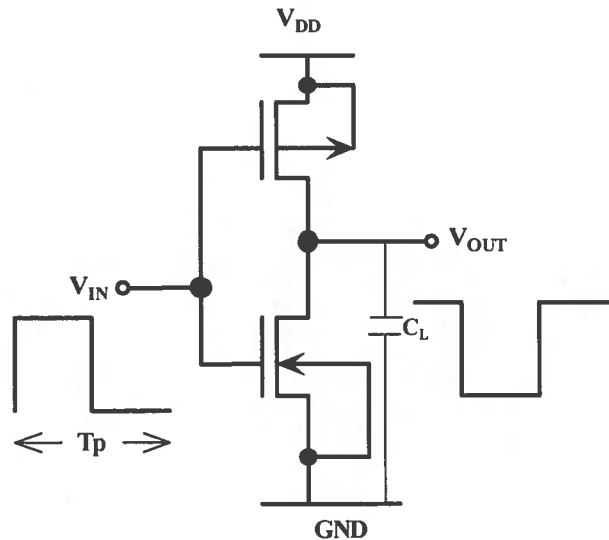
Given: $V_{DD} = 5V$

For n-MOSFET:	**For p-MOSFET:**
$\mu_n C_{OX} = 20 \ \mu A/V^2$	$\mu_p C_{OX} = 10 \ \mu A/V^2$
$W/L = 2$ and $V_{th,n} = 1V$	$W/L = 4$ and $|V_{th,p}| = 1V$

Where $V_{th,n}$ and $V_{th,p}$ are threshold voltages of n-and p-MOSFETs. L and W are channel length and gate width of the MOSFET. μ is the mobility of carriers in the channel region. C_{OX} is the gate gate oxide capacitance /area.

MOSFET I-V Relations:

$I_D = 0.5\mu C_{OX}(W/L)\{2(V_{GS}-V_{th})V_{DS}-V_{DS}^2\}$ (Linear region)

$I_D = 0.5\mu C_{OX}(W/L)\{(V_{GS}-V_{th})^2\}$ (Saturation region)

Where V_{GS} is the gate-to-source voltage and I_D is the drain current.

b) Compute dynamic power dissipation. Given $C_L = 0.01 \ pF$ and $T_P = 100 \ nS$.

Circuits and Systems
Problem 3

a) Convert the following logic into CMOS integrated circuit and show substrate body connections of all MOSFETs to the appropriate power supply voltages, i.e., V_{DD} and Ground. Label each transistor in your circuit. Write the truth table showing ON and OFF states of all transistors. **Note:** Number of driver transistors must be equal to the number of load transistors.

$$Y = \overline{\{(A+B).C\}}$$

b) Divide voltage transfer characteristics of a typical CMOS inverter in 5 separate regions for $\beta = 1$ where $\beta = \beta_n/\beta_p$. β_n and β_p are transconductance parameters of n- and p-channel MOSFETs, respectively. Write ON and OFF states and corresponding regions of operation of n- and p-channel MOSFETs in each section.

Circuits and Systems
Problem 4

Consider the op-amp circuit shown below. The individual bits of the 4-bit binary input word, $s_1\ s_2\ s_3\ s_4$, are used to controlled to position of the switches with the resistor connected to 0 V if $s_N = 0$ and connected to the input signal v_{IN} if $s_N = 1$. Resistors are $R_1 = 2R$, $R_2 = 4R$, $R_3 = 8R$, and $R_4 = 16R$, where R is a finite resistor.

(a) Find the output voltage v_{OUT} with the data input 0110 if $v_{IN} = 2\ \sin(4000\pi t)$ V.

(b) In (a), what will be the new output voltage if the input changes to 1011.

(c) Make a table giving the output voltages for all 16 possible input combinations.
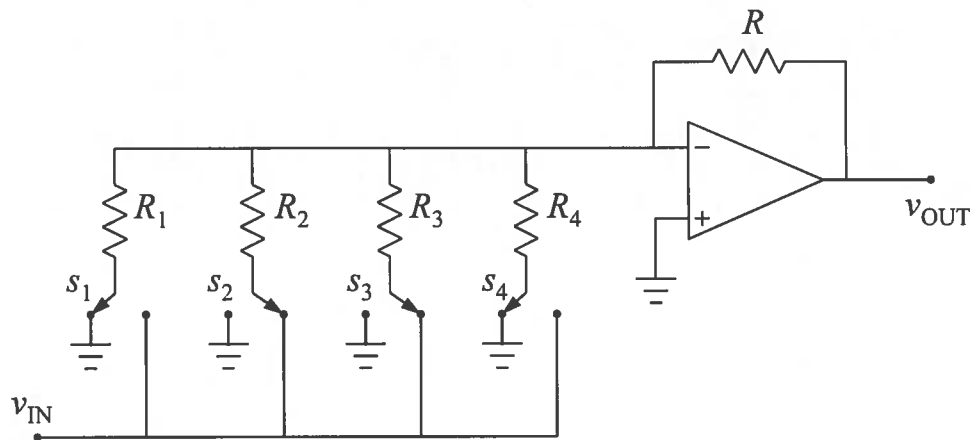
Circuits and Systems
Problem 5

For the amplifier circuit shown in the figure below,
a) Calculate the resistance values R_{C1}, R_{C2}, R_{C3}, R_{C4}, R_{EE1} and R_{EE2}.
Given: $V_{CC} = +15V$, $V_{EE} = -15V$, Transistor base-emitter voltage during conduction
$V_{BE(ON)} = 0.7V$.

For Q_1 and Q_2:   For Q_3 and Q_4:
$I_{C1} = I_{C2} = 0.1$ mA $I_{C3} = I_{C4} = 1$ mA
$V_{CB1} = V_{CB2} = V_{CC}/2$ $V_{CB3} = V_{CB4} = (V_{CC}-V_{B3})/2$
$\beta_F = \beta_0 = 50$ $\beta_F = \beta_0 = 50$

Here, β_0 is d.c. common-emitter current gain and β_F is forward small signal current gain.
V_{CBX} is the collector to base voltage and V_{BX} is base voltage of transistor Q_X.
b) Calculate the above resistance values if the supply voltages are now reduced to that
$V_{CC} = +6V$, $V_{EE} = -6V$.
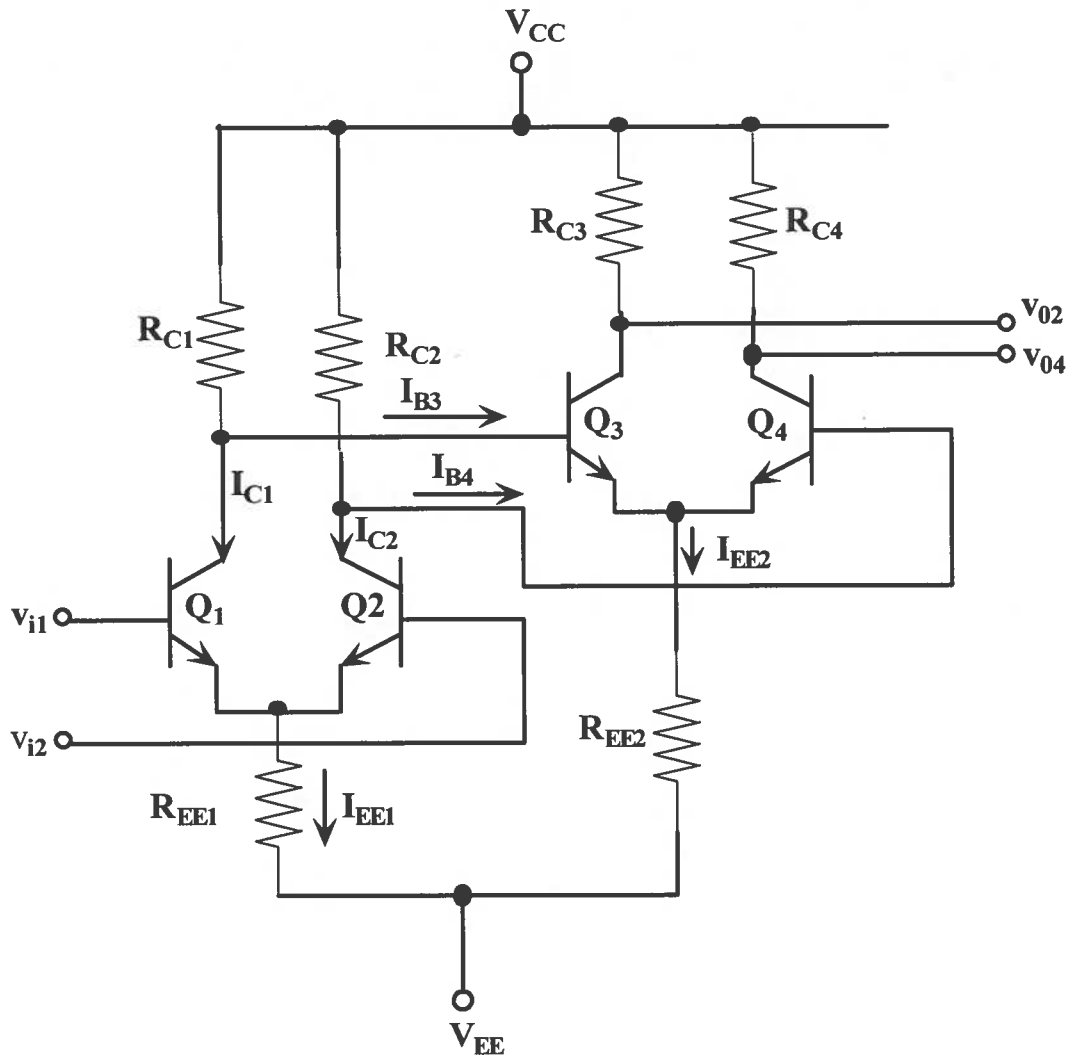
Circuits and Systems
Problem 5

Consider the op-amp circuit shown below. Given $0 < \delta < 1$. Assume an ideal op-amp and answer the following questions.

(a) Find a general expression for the output voltage, v_o.

(b) Find an expression for common mode rejection ratio (CMRR).

(c) When $R_1 = 10\ k\Omega$ and $R_2 = 100\ k\Omega$, estimate the resistance tolerance, δ, required for a guaranteed CMRR of 80 dB.
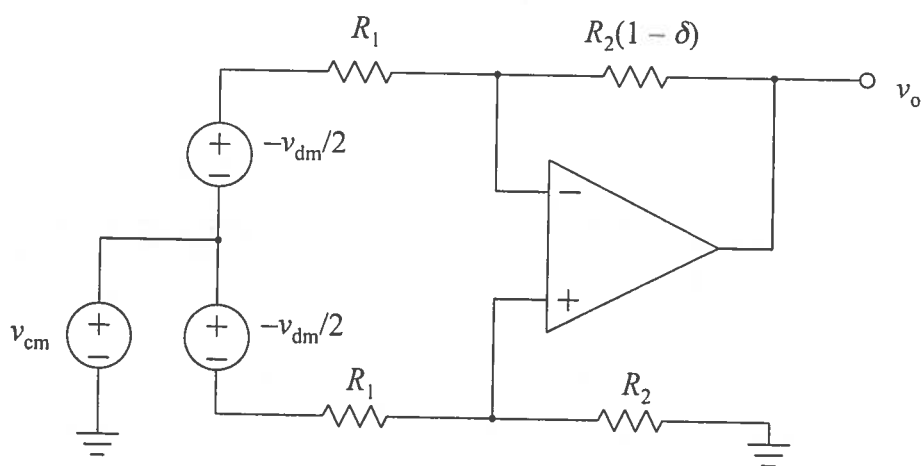
Physical Electronics
Problem 1

A silicon diode has the doping profile as shown in the figure below. N_D and N_A are donor concentration and acceptor concentration, respectively. Given,

$$p_0 = n_i \exp\left(\frac{E_i - E_F}{kT}\right) \quad \text{and} \quad n_0 = n_i \exp\left(\frac{E_F - E_i}{kT}\right)$$

where n_i is the intrinsic carrier concentration, E_i is the intrinsic Fermi level, E_F is the Fermi level, k is the Boltzmann constant and T is the temperature. n_0 and p_0 are electron and hole concentrations in equilibrium. x_n and x_p are n-side and p-side widths of the depletion region. Assume that $-x_p < -x_0$ for all applied biases of interest.

Impurity concentration
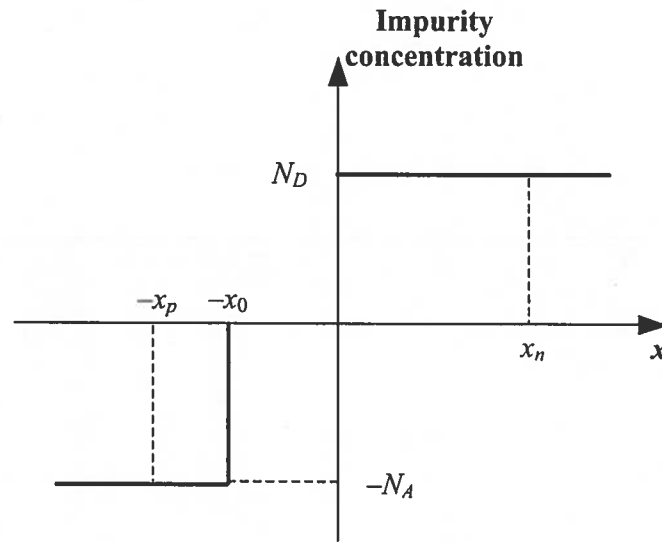
Given, $n_i = 1.45 \times 10^{10}$ cm^{-3}, $k = 1.38 \times 10^{-23}$ J/K, $T = 300$ K, $N_D = 5 \times 10^{15}$ cm^{-3}, $N_A = 1 \times 10^{16}$ cm^{-3}, and $x_0 = 0.5$ μm.

(a) Assuming impurities are 100% ionized, derive the expression for the built-in potential at thermal equilibrium. Justify your answer and show detailed steps.

(b) Calculate the built-in voltage (V_{bi}), x_n, and x_p.

(c) Draw an equilibrium band diagram.

(d) When a forward bias of 0.45 V is applied, repeat (b).

For a given cubic lattice, assume that each atom is a hard sphere. Let the surface of each atom is in contact with its nearest neighbor. Determine the percentage of total unit cell volume that is occupied in each of the following:

a) a simple cubic lattice

b) a face-centered cubic lattice

c) a body-centered cubic lattice

d) diamond lattice

Physical Electronics

Problem 2

The following schematic shows a PN junction, where p-type silicon is doped with a dopant concentration of N_a, and n-type silicon is doped with a dopant concentration of N_d. The thickness of the depletion region (or space-charge region) in p-type silicon is x_p, and that in n-type silicon is x_n.
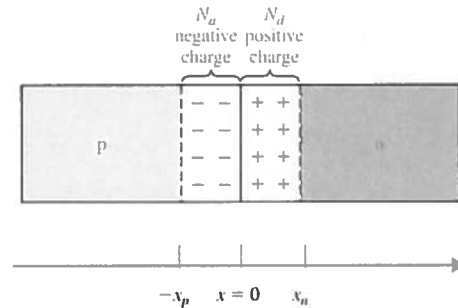

a) Draw the charge density of the pn-junction.

b) Draw the electric field in the pn-junction

c) Express the maximum intensity of the electric filed, using N_a, N_d, q, x_n, x_p, and ε_s. (q is unit charge, and ε_s is the permittivity of silicon) Where is the maximum intensity of the electric field located?

d) Express the built-in potential, V_{bi} in terms of N_a, N_d, q, x_n, x_p, and ε_s. (q is unit charge, and ε_s is the permittivity of silicon)

e) Express x_p in terms of N_a, N_d, q, V_{bi} and ε_s. (You can assume charge-neutrality and complete ionization of the dopant.)

Physical Electronics
Problem 3

Consider a silicon sample under light illumination with an intensity of $I_{v0} = 0.1$ W/cm^2 on the surface of the sample. Absorption coefficient for several semiconductor materials is shown in the graph below. The Planck constant, h, is 6.626×10^{-34} J-s.
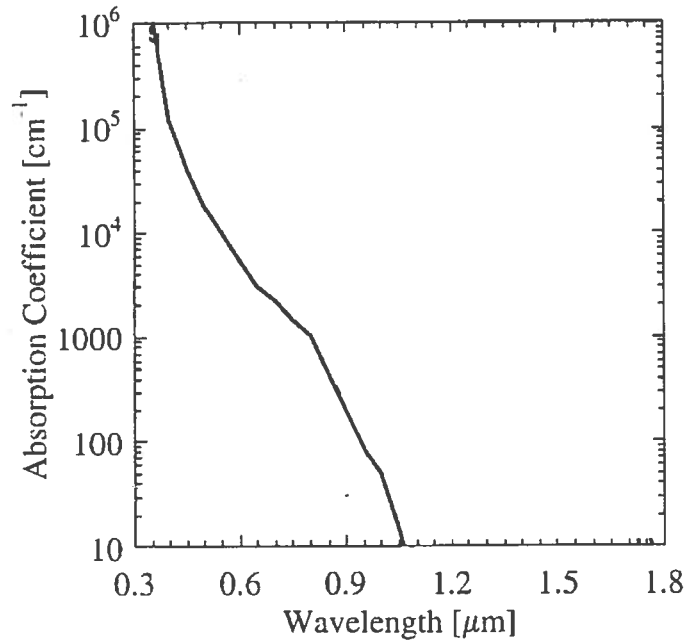
(a) When the wavelength of light is 1 μm, determine the photon flux intensity at a depth of 5 μm from the surface. Assume that the surface does not reflect the incident light and the ambient temperature is 300 K.

(b) Repeat (a) at a depth of 10 μm.

(c) Determine the generation rate of excess electron-hole pairs at depths of 5 μm and 10 μm from the surface.

(d) Discuss whether the answers found in (c) will be dependent on temperature or not. Provide the reasons for your answer.

The following is the minority carrier transport equation. (Each sub-question is not related to each other.)

$$D_n \frac{\partial^2(\delta n)}{\partial x^2} + \mu_n E \frac{\partial(\delta n)}{\partial x} + g' - \frac{\delta n}{\tau_{n0}} = \frac{\partial(\delta n)}{\partial t} \qquad \text{for p - type}$$

δn : Excessive minority carrier $\qquad D_N$: Diffusion coefficient

τ_n : Minority carrier life time $\qquad g'$: Photogeneration rate

1) What is μ_n? (answer in 2 words.)

2) At high electric field (E>100kV/cm), the velocity of the carrier is saturated to v_{sat}. Modify the minority carrier transport equation, to model the electron's velocity saturation and justify your answer. (The electron is assumed to move in +x direction.)

3) The distribution of the excess minority carrier at t = 0 is as below ($\delta n_0 > 0$).

$$\delta n(x)_{t=0} = \delta n_0 x(1-x) \qquad 0 \le x \le 1$$
$$\delta n(x)_{t=0} = 0 \qquad\qquad x < 0, \quad 1 < x$$

Will the excess minority carrier concentration (δn) at x=0.5 increase or decrease when t=0? Justify your answer. (You can assume that photo-generation rate is very low and that the minority carrier life time is very large.)

What is the electric field that will keep the minority carrier concentration (δn) constant at t=0 and x = 1/3? Justify your answer. (You cannot ignore the photo-generation rate and the minority carrier life time.)

Physical Electronics
Problem 5

The magnetic field in a sourceless region in free space is given by

$$\mathbf{H} = H_0 \sin\left(\frac{\pi y}{d}\right) e^{-j\beta z} \hat{\mathbf{x}}.$$

(a) Show that $\nabla \cdot \mathbf{H} = 0$.

(b) Find the electric field $\mathbf{E}$.

(c) Show that $\left(\dfrac{\pi}{d}\right)^2 + \beta^2 = \omega^2 \varepsilon_0 \mu_0$.

Physical Electronics
Problem 3

The figure below illustrates a semiconductor block for measuring the Hall effect. A current (I) is applied in $+y$ direction and a magnetic field (B) is applied in $+z$ direction. Answer the following questions.
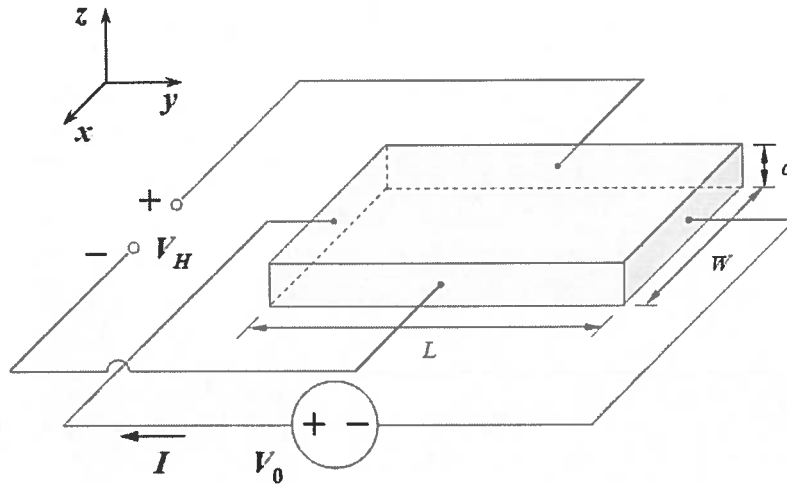
(a) Explain how the Hall effect can be used to distinguish the doping type of a semiconductor.

(b) Derive an expression of the Hall voltage V_H for a p-type semiconductor. Define parameters if necessary.

(c) Consider that the silicon Hall sensor whose geometry is $L = 1$ mm, $W = 50$ μm, and $d = 5$ μm in the figure shown above is placed in the known magnetic field (B). When $B = 50$ mT (or 0.05 Wb/m^2), $I = 1$ mA, and $V_0 = 5$ V, the measured Hall voltage (V_H) is 5 mV. Determine the type, concentration, and mobility of the majority carrier.

(d) Will the Hall voltage have temperature dependence? Present your view on this.

A. Develop power equation of the three-phase unbalanced linear-time invariant (LTI) load specified in terms of line-to-line admittances for harmonics Y_{RS}, Y_{ST}, Y_{TR}, assuming that the supply voltage is sinusoidal, but symmetrical and of the positive sequence.

B. Specify phenomena that affect the power factor of such loads.

C. Calculate the rms values of the active, reactive and unbalanced currents in the circuit shown in Figure and the power factor, λ, of the supply, assuming that $Z_R = 2+j3$ Ω.
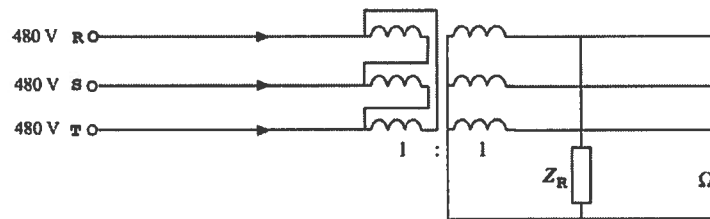
A Buck-Boost DC/DC converter supplied with voltage $U = 200$ V is used for the control of the output voltage on the resistance $R_0 = 15$ Ω from $U_1 = 100$ V to $U_2 = 300$ V. Draw the structure of the converter, the waveforms of the inductor and capacitor currents. Calculate inductance L and capacitance C of the converter if the switching frequency is equal to $f = 15$ kHz and output voltage ripples cannot be higher than 5 % of the output voltage.

Let (A, B, C, D) be a realization of order n, and A be a Schur stability matrix. Let P and Q be the observability and reachability gramians, respectively. That is,

$$P = A^T P A + C^T C, \quad Q = A Q A^T + B B^T.$$

1. Let $P = U \Sigma_o U^*$ be singular value decomposition where U is unitary, and Σ_o is diagonal and of rank $r_o < n$. Show that similarity transform $S = U^T$ yields observability Kalman decomposition.

2. Let $Q = V \Sigma_c V^T$ be singular value decomposition where V is unitary, and Σ_c is diagonal and of rank $r_c < n$. Show that similarity transform $S = V^T$ yields reachability Kalman decomposition.

3. Suppose that A is not a Schur stability matrix but satisfying $\lambda_i(A)\lambda_k(A) \neq 1$ for all (i, k). In this case the two Lyapunov equations still have unique solutions P and Q. Can you use the same method as 1. and 2. for finding the Kalman decompositions? Why or why not?

Consider a linear system with the following state space realizaiton

$$\dot{x} = \begin{bmatrix} -1 & 0 \\ 0 & 2 \end{bmatrix} x + \begin{bmatrix} 0 \\ a \end{bmatrix} u$$
$$y = \begin{bmatrix} b & 1 \end{bmatrix} x$$

1. Determine the condition for the controllability and the stabilizability of the system.

2. Determine the condiiton for the observability and detectability of the system.

3. Let $a = 1$. Find a state feedback $u = Fx$ if possible so that the closed eigenvalues are at -1 and -10. Find another state feedback if possible so that the closed eigenvalues are at -10 and -10.

4. Let $a = 1$ and $b = 0$. Find a state estimator (or observer) so that the states can be asymptotically estimated.

Let a transfer matrix be given by

$$
G(s) = \begin{bmatrix} \dfrac{1}{s+1} & \dfrac{10(s+5)}{s(s+1)} \\[3mm] \dfrac{1}{s+2} & \dfrac{20}{s} \end{bmatrix}
$$

1. Find a minimal (controllable and observable) realization for G.

2. Find a Smith-McMillian form for the transfer matrix G.

3. Find the transmission zeros of the system.

4. Suppose z is a zero. Then find a vector $u = \begin{bmatrix} 1 \\ a \end{bmatrix}$ so that $G(z)u = 0$.

Consider a unity feedback system with open loop transfer function

$$G(s) = \frac{K(s-1)}{s(s-2)(s+10)}$$

1. Draw root locuses for $K > 0$ and $K < 0$ respectively.

2. Show that the feedback system cannot be stabilized by any stable controller.

3. Suppose $C(s)$ is a controller that stabilizes the feedback system. Discuss the possible controller poles and zeros locations.

For a unity negative feedback control system, the open loop system is given by

$$KG(s) = \frac{K(s+2)(s-1)}{s^2(s+9)}.$$

1. Use Routh-Hurwitz method to find the range of K for which the feedback system is stable.

2. Sketch the Nyquist plot, and find range of K that makes the feedback system stable.

3. Sketch the zero-degree root locus to validate the result in the previous two parts.

Consider a unity negative feedback system with a plant model given by

$$P(s) = \frac{10}{s-1}$$

and a controller given by

$$C(s) = \frac{s+b}{s}$$
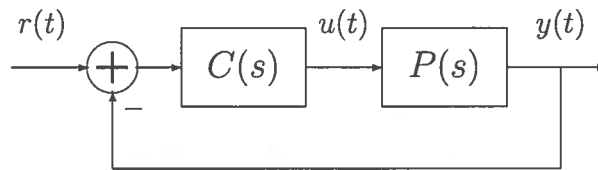
for some real parameter b.

Fig. 1 Feedback control system

1. Write a state space realization of the feedback system.
2. Find the closed-loop transfer function from r to y when $b = -1$. Is the system bounded input and bounded output stable from r to y?
3. Discuss the closed-loop stability, controllability, and observability when $b = -1$.
4. Discuss the closed-loop stability, controllability, and observability when $b = 5$.

Let a transfer matrix be give by

$$G(s) = \begin{bmatrix} \dfrac{1}{s-1} & \dfrac{1}{s} \\ 0 & 1 \end{bmatrix}$$

1. Find a minimal (controllable and observable) realization for G.
2. Find a Smith-McMillian form for $G(s)$.
3. Find the poles and the transmission zeros of the system.
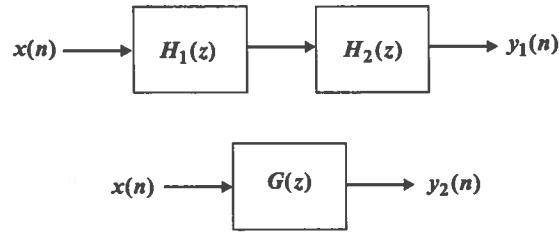
The above figure depicts two linear time-invariant causal systems. Assume that $G(z) = H_1(z) H_2(z)$ is always true, and $G(z)$ is of irreducible form (no common factor between numerator and denominator polynomials) and represents a bounded-input bounded-output (BIBO) stable system. Some pole(s) of $H_1(z)$ would be allowed to be outside the unite circle of the z-plane. The discrete-time Fourier transforms (DTFTs) of the output signals $y_1(n)$ and $y_2(n)$ are denoted by $Y_1\left(e^{j\omega}\right) = \sum\limits_{n=-\infty}^{\infty} y_1(n) e^{-j\omega n}$ and $Y_2\left(e^{j\omega}\right) = \sum\limits_{n=-\infty}^{\infty} y_2(n) e^{-j\omega n}$, respectively, where $j = \sqrt{-1}$.

1. Is it true that we will always obtain $y_1(n) = y_2(n)$ no matter what kind of bounded input $x(n)$ we apply? Justify your answer in rationale.

2. Use a particular example here. Assume that $G(z) = \frac{Kz}{z-\beta}$, where β is a real number and $|\beta| < 1$. Construct $H_1(z) = \frac{z}{z-\gamma}$ and $H_2(z) = \frac{K(z-\gamma)}{z-\beta}$, where γ, K are real numbers and $\gamma \neq \beta$, $K \neq 0$. Use these transfer functions to implement the causal systems depicted above. What is the restriction on γ to guarantee the BIBO stability of the cascade system? What is the restriction on γ to guarantee $y_1(n) = y_2(n)$ for any arbitrary bounded input signal $x(n)$?

3. A system transfer function, say $H_1(z)$, which has some pole(s) outside the unite circle of the z-plane, obviously cannot represent a *causal stable system*. How do we build a *compensator* $H_2(z)$ such that $G(z) = H_1(z) H_2(z)$ where $G(z)$ represents a causal stable system and the corresponding output magnitude spectra satisfy $|Y_1\left(e^{j\omega}\right)| = |Y_2\left(e^{j\omega}\right)|$, for all ω?

The 4-PAM (pulse amplitude modulation) alphabet $\mathcal{A} = \{\pm 1, \pm 3\}$ might be called *unfair* in the sense that some symbols are more likely to be decoded erroneously than others. In other words, the conditional error probability $P(\text{error}|a)$ depends on which symbol a is transmitted. The goal of this problem is to modify 4-PAM to make it fair, in the sense that the conditional error probability $P(\text{error}|a)$ does not depend on which symbol a is transmitted. Consider a new 4-ary alphabet $\mathcal{A}' = \{\pm 1, \pm 3\beta\}$, where the parameter β determines how far to move the outer points. This alphabet reduces to the conventional 4-PAM alphabet when $\beta = 1$.

1. In the presence of additive white Gaussian noise (AWGN) with maximum like-lihood (ML) detection, is $P(\text{error}|a = \pm 1)$ larger or smaller than $P(\text{error}|a = \pm 3)$? Explain.

2. Does there exist a real value for the parameter β such that fairness is achieved, in the sense that $P(\text{error}|a = \pm 1) = P(\text{error}|a = \pm 3\beta)$? If necessary, assume that signal-to-noise ratio (SNR) is 4 dB.

3. If yes, specify the value of β that achieves fairness. If no, explain why it is impossible.

Let X and Y be statistically independent and identically distributed (i.i.d.) random variables $\sim \mathcal{N}(0, 1)$ (Gaussian with zero mean and unit variance). Let $W = X + Y$, and let $V = X + \sin(\theta)Y$, where θ is a constant.

1. Find the expectations of W, V, and WV.

2. Find a numerical value for the constant θ in the range $-\pi \leq \theta \leq \pi$ so that W and V are uncorrelated.

3. Find a numerical value for the constant θ in the range $-\pi \leq \theta \leq \pi$ so that W and V are statistically independent.

Consider a Gaussian channel with binary input $x \in \{-1, +1\}$ and real output alphabet $\mathcal{A}_y$, with transition probability given by

$$f(y|x, \alpha, \sigma) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(y-x\alpha)^2}{2\sigma^2}}$$

where α is the signal amplitude.

1. Compute the probability of x given y, assuming that the two inputs are equally likely. Put your answer in the form

$$P(x = 1|y, \alpha, \sigma) = \frac{1}{1 + e^{-g(y)}}$$

where $g(y)$ is a function of y.

2. Assume that a single bit is to be transmitted, and the two inputs are equally likely. What is the optimal decision rule to determine $\hat{x} \in \{1, -1\}$ based on y, and what is the probability of error $P_e(\alpha, \sigma)$? Express your answer in terms of the signal to noise ratio α^2/σ^2, and the Q function: $Q(x) = \int_x^\infty \frac{1}{\sqrt{2\pi}} e^{-\frac{z^2}{2}} \, dz$.

3. If α is an unknown random variable uniformly distributed over an interval $[0, 1]$, find the new decision rule for $\hat{x} \in \{1, -1\}$, under the same assumption of equal prior probabilities. To evaluate the resulting average error probability, can we integrate the average error probability $P_e(\alpha, \sigma)$ obtained in the second part over the density function of α given here? Justify your answer.

Assume that X_n is a wide-sense stationary random sequence with autocorrelation function $R_X[k] = E[X_n X_{n+k}]$, where n and k are integer-valued discrete-time variables. The random sequence Y_n is obtained from X_n by $Y_n = X_n + \beta^n X_{n-1}$, where $\beta \neq 0$ is a real-valued constant.

1. Find the autocorrelation function of Y_n.

2. Find the cross-correlation function of X_n and Y_n.

3. Determine those values of β for which Y_n is wide sense stationary.

4. Determine those values of β for which X_n and Y_n are jointly wide sense stationary.

The unit-step input signal $u(n)$ is defined as 1 for $n \geq 0$ and 0 for $n < 0$. Consider a causal, linear and time-invariant (LTI) system whose input signal is given by $x(n) = u(n-1)$ and whose output signal is given by

$$y(n) = 2^n u(-n-2) - (1/5)^n u(n-1).$$

1. Determine the impulse response $h(n)$ of this LTI system.

2. Find the transfer function $H(z)$.

3. Determine whether the LTI system is stable or not, in a bounded-input bounded-output (BIBO) sense.

4. If the LTI system has the input signal $x(n) = 3^n u(n) + u(-n)$, determine the corresponding output signal $y(n)$.

Let the random process $Y(t)$ be given by

$$Y(t) = X(t) - 2\frac{dY(t)}{dt},$$

where $X(t)$ is a random process with mean function $\mu_X(t) = 5t$, and the covariance function

$$C_{XX}(t_1, t_2) = \frac{1}{1 + (t_1 - t_2)^2}.$$

1. Find the mean function $\mu_Y(t)$.

2. Find the covariance function $C_{YY}(t_1, t_2)$.

3. Is the random process $Y(t)$ wide sense stationary? Why?

A single binary equally-likely message is to be transmitted across a filtered additive white Gaussian noise (AWGN) channel. The frequency response of the channel filter is given by $H_c(f) = \text{sinc}(f) = \frac{\sin(\pi f)}{\pi f}$. The channel noise power spectral density is given by $S_{N_W}(f) = N_0/2$.

The following signal set is used to transmit a single message across the channel.

$$\mathcal{S} = \{s_0(t), s_1(t)\}$$

where $s_1(t) = -s_0(t)$ and where

$$s_0(t) = \begin{cases} 1, & 0 < t < 2 \\ 0, & \text{otherwise.} \end{cases}$$

1. Sketch the block diagram of the minimum probability of error receiver for this signal set. You must clearly describe the function of each block.

2. Find the probability of error for your receiver.

At a casino, people line up to pay \$20 each to be a contestant in the following game: The contestant flips a fair coin repeatedly. If he/she flips head 20 times in a row, he/she walks away with $R = 20$ million dollars; otherwise, then walks away with $R = 0$ dollars.

1. Find the probability mass function (PMF) of R, the reward earned by the contestant, and draw its corresponding cumulative distribution function (CDF) $F_R(r)$.

2. Compute $E[R]$, the average of R, and what is the average of net gain of the contestant, considering the cost of each ticket?

3. The casino counts "losing contestants" who fail to win the 20 million dollar prize. Let L equal the number of losing contestants before the first winning contestant. What is the PMF of L?

4. Why does the casino offer this game?

5. If a player questions the fairness of this game in terms of the biasness of the "fair" coin, what kind of procedure you would recommend to test if the coin is fair or not, please justify your answer.

Consider a system whose input is $x(t)$, and corresponding output is $y(t)$, answer the following questions with your justification.

1. If $y(t) = x(2t)$, is this system time-invariant? What is the relationship between the input Fourier transform $X(j\omega)$ and output Fourier transform $Y(j\omega)$? Can we have a properly defined impulse response $h(t)$ for such a system?

2. For another system, which is linear and time invariant, if its input is $\delta_\Delta(t) = \frac{1}{\Delta}[u(t) - u(t - \Delta)]$, where $u(t)$ is the unit step function, the corresponding output is denoted as $h_\Delta(t)$. For any other bounded input $x(t)$, provide an approximation $\tilde{x}(t)$ of $x(t)$ using $\delta_\Delta(t)$ and its scaled and shifted transformations. What is the resulting output of the same system for such an input $\tilde{x}(t)$?

3. If the relationship between $x(t)$ and $y(t)$ is characterized by a first order differential equation $\frac{dy(t)}{dx(t)} + ay(t) = x(t)$, where $a \neq 0$ is a real number, what is the constraint on a so that the system is bounded?

4. For a bounded system governed by the above differential equations under a particular a_0, if the input $x(t)$ is a zero mean white Gaussian random process whose power spectral density (PSD) is $N_0/2$ over the entire frequency domain, is the output process $y(t)$ also second order stationary? If yes, what is the resulting PSD? Can we sample $y(t)$ at $t_1 \neq t_2$, respectively, so that $y(t_1)$ and $y(t_2)$ are statistically independent?