MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

AUTOMATIC CONTROL TOPICS

A. Basic Tools
Laplace, Z transforms: basic properties, use in solving linear differential/difference equations, application to system analysis, transfer functions. Fourier transform, Fourier series: basic properties, application to signal analysis, frequency response, spectral energy density.

B. Basic Concepts
Linearity, time invariance, causality, difference and differential systems, linearization, signal-flow and block diagrams, BIBO and asymptotic stability.

C. Classical Control
Transient and steady state analysis and performance indicators, pole location, sensitivity; frequency domain analysis, phase and gain margins; Nyquist stability, Routh-Hourwitz criterion, root locus, lead and lag compensator design, PID control; pole placement with fractional controllers.

D. Sampled Data Systems
Basic A/D and D/A conversion, sampling theorem. Discretization of continuous time systems, deadbeat control.

E. State Space Control for Continuous and Discrete Time Systems
State and state equations, transition matrix, solution of state equation. Realization, controllability and stabilizability, observability and detectability, Lyapunov stability, state feedback and pole placement, asymptotic observers, state feedback with observers.

Representative References

1. C-T. Chen, *System and Signal Analysis*, Saunders College Publishing.
2. B.C. Kuo, *Automatic Control Systems*, Prentice Hall.
3. G.F. Franklin, J.D. Powell, A. Emami-Naeini, *Feedback Control of Linear Systems*, Addison Wesley.
4. G.F. Franklin, J.D. Powell, M.L. Workman, *Digital Control of Dynamic Systems*, Addison Wesley.
5. K. Ogata, *Discrete-time Control Systems*, Prentice Hall.
6. W.L. Brogan, *Modern Control Theory*, Quantum Publishers, Inc.
7. T. Kailath, *Linear Systems*, Prentice Hall.
8. K. Ogata, *Modern Control Engineering*, Prentice Hall.
9. C. T. Chen, *Linear system Theory and Design*, 3rd Ed., Oxford University Press, 1999.

M.S. Comprehensive /Ph.D. Qualifying Exam
Communication and Signal Processing Topics

Probability Theory and Random Processes
Basic concepts in probability theory; stationarity and wide sense stationarity of random processes, power spectral density, linear filtering of random processes, minimum mean squared error estimation, Gaussian and Poisson random processes.

Signals, Systems, and Digital Signal Processing
Continuous time and discrete time signals and systems: fundamental concepts, system properties (causality, stability, time invariance, etc.); time and frequency domain characterization of discrete and continuous time signals and systems; transform domain techniques; sampling and reconstruction; sampling rate conversion, frequency-domain analysis, aliasing and Nyquist rate concepts; discrete Fourier Transform and FFT algorithms; design and implementation of FIR and IIR filters.

Analog Communication
Amplitude modulation techniques; frequency and phase modulation techniques; sampling, quantization; pulse code modulation (PCM); effect of noise on continuous wave and PCM systems.

Digital Communication
Signal space representation; baseband representation of bandpass signals and systems; maximum likelihood (ML) detection and estimation; optimum receiver principles. performance of optimum receivers; differential, partially coherent and non-coherent detection of signals; bandwidth efficiency and power efficiency; receiver design and performance analysis of digital modulation schemes in fading channels; linear block codes and their decoding strategies, hard decision and soft decision decoding.

Representative References

1. Simon Haykin, *Communications Systems*, (Wiley).
2. J. G. Proakis and M. Salehi, *Communication Systems Engineering, 2nd Edition*, Prentice Hall.
3. J. G. Proakis, *Digital Communication*, 4th Edition, McGraw-Hill, 2000.
4. J. M. Wopzencraft and I. M. Jacobs, *Principles of Communication Engineering*, John Wiley & Sons, New York, 1965.
5. Henry Stark and John W. Woods, *Probability and Random Processes with Applications to Signal Processing, 3rd Edition.* Prentice-Hall.
6. *Probability, Random Variables, and Stochastic Processes*, A. Papoulis, 3rd edition, McGraw-Hill, 1991.
7. S. K. Mitra, *Digital Signal Processing*, 3rd edition, McGraw-Hill.
8. A. V. Oppenheim and R.W. Schafer, *Discrete-time Signal Processing*, Prentice-Hall.

MS COMPREHENSIVE / PHD QUALIFYING EXAM

COMPUTER ENGINEERING TOPICS

Appearing below is an outline of topics which computer-area questions will be based on. Most of the topics clearly fall into one of the three question areas, Hardware, Software, and Applications, but questions in one area can draw on topics from other areas. For example, the solution to an algorithm (software) question might require knowledge of cache organization (hardware).

Topics described with "Proficiency in" (or similar wording) must be understood very well, as though you were going to take a test in a course covering the topic. Topics described using "Competence with" (or similar wording) must be understood well enough to solve problems or answer substantive questions, however definitions or other background might be provided as part of the question. This information should help students that know the material make a quick start solving the problem. For topics listed under "Familiarity with" students should have a basic background in the area, including basic terminology, but need not know many specifics. For these problems a greater amount of background will be provided, enough so that a good student might be able to solve them without having taken any courses covering the topic.

Logic Design
Proficiency with combinational and sequential logic theory at EE 2720 and EE 2730 level, including Boolean algebra and basic minimization techniques. Proficiency in designing basic combinational and sequential circuits.

Computer Arithmetic
Proficiency with signed integer representations and with full adder and carry look-ahead adder designs. Competence with basic integer multiplication and division circuits. Competence with floating-point (FP) representations, including IEEE 754, and with FP arithmetic. Familiarity with modular and residue arithmetic.

Computer Instruction-Set Architecture (ISA) and Microarchitecture
Proficiency with 5-staged pipelined RISC (e.g., MIPS) implementations, including design rationale, direct and bypassed data paths, control signals, and relationship between implementation and instructions. Competence in assembly language programming, including RISC instruction sets. Competence with instruction set design issues, including memory addressing modes, and the variety of jumps & branch instructions. Familiarity with interrupts, traps, and exceptions. Familiarity with pipeline depth and superscalar width issues. Familiarity with caches and branch prediction techniques.

Computer Communication Networks
Competence with basic switching and multiplexing techniques. Familiarity with network layers and protocol stacks, ARQ protocols, error detection and correction. Familiarity with Internet addressing and routing standards and techniques. Familiarity with network reliability, availability, structural reliability terminology and techniques.

Algorithms and Data Structures
Proficiency with basic data structures (including arrays, stacks, linked lists, trees), basic algorithms (including binary search, merge sort, tree searches), memory content and layout of numbers, pointers, arrays, and structures complexity analysis of algorithms. Competence with advanced data structures (including hash tables, graph representations), algorithmic paradigms (including divide and-conquer, greedy, dynamic programming) and analysis techniques (including recurrence relations, amortized analysis). Familiarity with computational complexity and intractability randomized, online and approximation algorithms.

Parallel and Distributed Computing
Competence in major parallel system organization topics including hardware organizations (CPU & network), parallel program organizations (processes, tasks, or threads), communication models (message passing or shared memory). Competence with metrics for analysis of performance including speedup, efficiency, time complexity, and space complexity. Competence with use and implementation of basic synchronization primitives and constructs including compare & swap, atomic memory operations, semaphores, and barriers. Competence with basic parallel algorithms including reduction, sorting, leader election, graph algs, etc. Competence with common interconnects including bus, crossbar, mesh, hypercube networks.
Familiarity with other interconnects including Log n stage networks (e.g., omega), Clos and Benes networks.

Operating Systems and Compilers
Competence with coordination concepts, constructs, and issues, including multiple-process access to shared structures, mutual exclusion, and deadlock. (See also basic synchronization topics under Parallel and distributed computing.) Competence with basic memory management issues including virtual and physical addresses and their rationale virtual to physical address translation techniques, page swapping basics. Competence with program compilation techniques, including control-flow and data-flow program representations, dependencies and dependence testing, common optimizations, and common program transformations.

Computer Vision and Image Processing
Proficiency in geometric and radiometric image formation. Proficiency in image segmentation, enhancement and restoration techniques. Competence in image compression and morphological image processing. Familiarity with pattern recognition techniques.

Logic Testing and Reliability
Familiarity with fault models, including the stuck-at model.

March 4, 2010

MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

ELECTRONICS ENGINEERING TOPICS

A.   Circuits

Circuit applications of diodes.   Circuit applications of BJT, MOSFETs and JFETs in linear and digital circuits.   Linear applications include amplifiers, oscillators, differential amplifiers and operational amplifiers.   Applications of ideal operational amplifiers.   Digital applications include internal operation of standard logic gates used as building blocks in logic families such as TTL, ECL, NMOS and CMOS.

B.   Devices

Basics of carrier transport in semiconductor materials, physics of p-n junction diodes, bipolar and field effect transistors.   Derivation of terminal current-voltage characteristics of discrete devices, large and small signal models. Basic physics of photonic devices.   Basic integrated circuit technology.

C.   Fields

Static fields, Maxwell's equations, propagation through istropic medium, reflections and basic antenna theory.

Representative References

1. M.N. Horenstein, *Microelectronic Circuit and Devices*, Prentice Hall.
2. Mitchell & Mitchell, *Introduction to Electronic Design*, 2nd Ed., Prentice Hall.
3. Gray & Mayer, *Analysis and Design of Analog Integrated Circuits*, 3rd Ed., John Wiley.
4. D. A. Hodges, H. G. Jackson and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, 3rd Ed., McGraw-Hill.
5. B. Streetman, *Solid State Electronic Devices*, 3rd Ed., Prentice Hall.
6. J.P. McKelvey, *Solid State and Semiconductor Physics*, Harper & Row.
7. Shen, *Applied Electromagnetics*, 2nd Ed., Prindle-Weber-Schmidt.

COMPREHENSIVE MS/QUALIFYING PH.D. EXAM

POWER ENGINEERING TOPICS

A. Electric Machinery
    Maxwell's equations; analysis of simple electromechanical devices using Maxwell's equations; synchronous machines, voltage behind reactance model, Park transformation, d,q equations; exact and approximate equivalent circuits of single-phase transformers, nonlinear effects; modeling and calculation of its parameters of transmission lines; modeling and analysis of direct current and induction machines.

B. Power Systems
    Per-unit calculations; symmetrical components; sequence impedances of transformers, synchronous machines and induction motors, sequence impedances and capacitances of transmission lines; sequence networks for fault analysis; shunt faults (3-phase, LG, LLG, LL faults); series faults (1LO, 2LO); power flow equations, (Decoupled) Newton-Raphson, Gauss/Gauss-Seidel methods; optimal dispatch with/without line losses; transient stability, swing equation, equal area criterion, effect of clearing time; low-frequency oscillations, supplementary excitation/governor control; linear optimal stabilization.

C. Power Electronics
    Fourier series of nonsinusoidal voltages and currents; analysis of circuits with nonsinusoidal voltage and current waveforms, nonsinusoidal active and apparent powers; single-phase and three-phase rectifiers, controlled AC/DC converters, DC/DC converters, inverters.

Representative References

1. R.D. Schultz & R.A. Smith, *Introduction to Electric Power Engineering,* John Wiley, 1988.
2. V. DelToro, *Electric Power Systems*, Prentice Hall, 1992.
3. P.M. Andersen, *Analysis of Faulted Power Systems*, The Iowa State Univ. Press, 1983.
4. Y.N. Yu, *Electric Power System Dynamics*, Academic Press, 1983.
5. M.H. Rashid, *Power Electronics*, Prentice Hall, 1988.
6. N. Mohan, T.M. Undeland, W.P. Robbins, *Power Electronics*, John Wiley, 1989.

This question is regarding to cache design.

(a) For the same cache size, is it possible for a direct-mapped cache having a better hit rate than a fully associative cache? If so, give an example for the access pattern or the program using the caches; if not, justify the reason.

(b) For the same cache with different replacement policies, is it possible for the cache with the least-recently-used (LRU) policy having a better hit rate than the optimal (OPT) replacement policy? If so, give an example for the access pattern; otherwise, explain why not?

(c) For a dual-core processor, there is a shared last level cache between the two cores. Two threads (T1 and T2) can run either individually or simultaneously. When the threads running individually, the last level cache hit ratio for the two threads (T1 and T2) are H1 and H2 respectively. When the threads running simultaneously, the last level cache hit ratio for the two threads (T1 and T2) is H1' and H2' respectively. Is it possible for H1' > H1 and H2' > H2? If yes, list an example for the access patterns or write the programs; otherwise, justify your answer.

Usually, we have two policies for memory disambiguation in an out-of-order executed processor: (1) a conservative solution is stalling a load instruction and its dependent instructions until the early store's address generation; (2) another alternative is predicting the memory dependence between loads and earlier outstanding stores. Memory dependence prediction allows loads to bypass earlier stores if no dependence is predicted. Otherwise, if dependence is predicted, load values can be forwarded from the latest earlier stores without cache access. At the commit stage of stores, the processor check correctness of predictions, if not, loads and their dependent instructions would be re-executed.

Now consider a two-issue, out-of-order execution pipeline with following stages: Instruction Fetch (IF), Decode (ID), Issue (IS), Execution / Address Generation (EX), Write Result (WR), Commit (CT). There are two integer ALU units, two load/store units and one MUL unit.

For the following code section, the EX stage for MUL instructions requires 10 cycles. All other instructions' EX stages have only 1 cycle. Please note that SW instructions only write cache in CT stage.

1. MUL	R2, R11, R12
2. SW	R1, 0(R2)
3. LW	R3, 20(R4)
4. ADD	R5, R3, R6
5. LW	R7, 100(R8)
6. SUB	R9, R7, R8
7. ADDI	R10, R5, 20

(a) If this pipeline employs the policy (1) mentioned above for memory dependence, show execution steps with timing for the above code section.

(b) If this pipeline employs the policy (2) mentioned above for memory dependence, the memory dependence predictor predicts that there is no dependence for both loads. Two loads (inst. 3 and 5) are executed without stalls. However, after the store address generation, instruction 3 has a true dependence with instruction 2 but instruction 5 doesn't have, show execution steps with timing for the above code section.

(c) Design a memory dependence predictor. The predictor would provide two predictions: dependence, no dependence. Draw a diagram for your design and specify the circumstances for each prediction.

Let $*$ be any associative binary operation. The *prefix computation* (with respect to $*$) on an array $A = \langle a_0, a_1, \cdots, a_{n-1} \rangle$ produces a second array $B = \langle b_0, b_1, \cdots, b_{n-1} \rangle$, where $b_i = a_0 * a_1 * \cdots * a_i$, for any $0 \le i < n$. The figure below shows prefix computation circuits for $n = 4$ and 8. In these figures, each box represents hardware for applying $*$ to its two inputs.
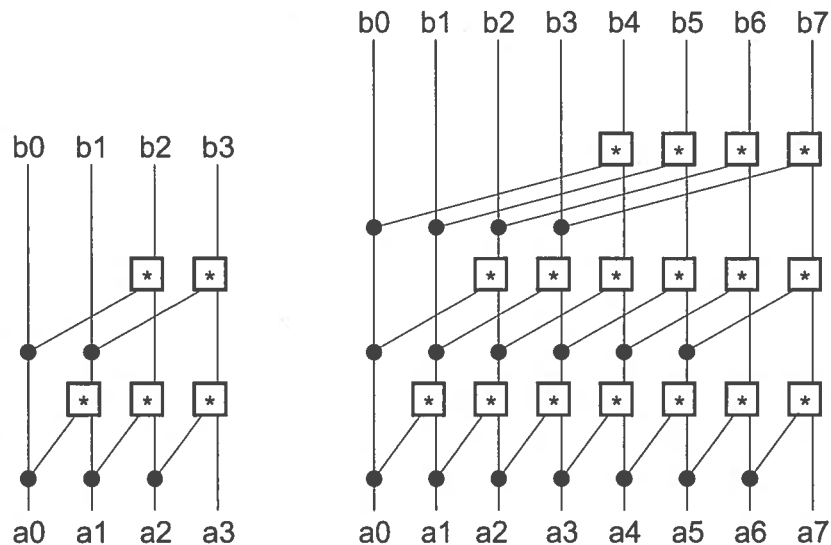

(a)   Draw a similar prefix computing circuit for 16 inputs.

(b)   Adapt the given circuit for 8 inputs to work for 5 inputs.

(c)   Describe the circuit for the general case of $n = 2^k$ inputs, and prove that it correctly performs the prefix computation.

(d)   Observe that adding 1 to an n-bit number amounts to complementing all lower order bits up to the first 0. For example, $10110\ 0111111 + 1 = \overbrace{10110}^{\text{unchanged}}\ \underbrace{1000000}_{\text{complemented}}$.

An n-bit binary counter counts up from 0 to $2^n - 1$ and then back to 0. Describe how a fast prefix computing circuit can help build a fast counter.

(a) "In the field of computer science, a binary decision diagram (**BDD**) or a propositional directed acyclic graph (PDAG) is a data structure that is used to represent a Boolean function The data structure is created using the *Shannon expansion* where a switching function is split into two sub-functions (cofactors) by assigning one variable (cf. *if-then-else normal form*). [Wikipedia]."
For example, the BDD for an AND gate with inputs x1 and x2 is as follows:
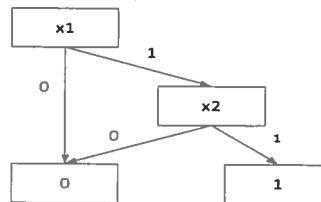
BDD for a 2-input AND gate

Using this concept, show the BDD for a (i) 2-input OR gate with inputs x1 and x2 and (ii) 1-bit Full Adder with inputs A_i, B_i, and C_{in} and outputs S_i and C_{out}.

(b) In the figure shown above (BDD for a 2-input AND gate), if each event (x_i as 1 or 0) is equally likely, find the probability of (a) output being 1 and (b) output being 0. What will happen to (b) if the probability of x_i being 1 changes to ¾ ?

Let $G = (T, E)$ be an undirected task graph, where T corresponds to a set of tasks and an edge $(i, j) \in E$ if tasks t_i and t_j communicate. Each edge (i, j) has a weight $c(i, j)$ denoting the volume of communication between t_i and t_j. For an $m \times m$ mesh of cores, some tasks $P \subseteq T$ have been mapped to cores. Two arrays describe this mapping. Array *map_by_place*$(g, h) = i$ means that core (g, h) has task t_i mapped to it; *map_by_place*$(g, h) = $ NIL means (g, h) is free. Array *map_by_task_ID*$(i) = (g, h)$ means that task t_i has been mapped to core (g, h); *map_by_task_ID*(i) = NIL means t_i has not been mapped.

(a) Design an algorithm to select the task in $T - P$ with largest communication volume to tasks in P.

(b) Design an algorithm to map the task selected in part (a) to a free core in M such that overall communication cost is minimized. (For task t_i mapped to core (r, s) that communicates with task t_j mapped to core (g, h), the *communication cost* is $c(i, j) * [\, |\, r - g\,| + |\, s - h\,|\,]$. The overall communication cost for task t_i is the sum of these communication costs between t_i and all tasks in P with which it communicates.)

(c) Derive the time complexity of the algorithms in parts (a) and (b). Let $n = |\, T\,|$, and let $q = |\, P\,|$.

Let $A = \langle a_1, a_2, \cdots, a_n \rangle$ be an array of n numbers. For the purpose of the following definition, assume that $a_0 = a_{n+1} = -\infty$. Define array A to be *positive unimodal* if and only if there is an index $1 \leq i \leq n$ such that $a_0 < a_1 < \cdots < a_{i-1} < a_i > a_{i+1} > \cdots > a_n > a_{n+1}$. A positive unimodal array has a unique local and global maximum. The array is *negative unimodal* if and only if the above conditions hold with $<, >$ exchanged and $a_0 = a_{n+1} = \infty$. A negative unimodal array has a unique global and local minimum. The array is *bimodal* if and only if there is an index $1 \leq j \leq n$ such that one of the two arrays $A_1 = \langle a_1, a_2, \cdots, a_j \rangle$ and $A_2 = \langle a_j, a_{j+1}, \cdots, a_n \rangle$ is positive unimodal and the other array is negative unimodal. A bimodal array has a local and global maximum and a local and global minimum.

Answer the following questions. All answers must be justified.

(a)   Give an example of each of positive unimodal, negative unimodal and bimodal arrays.

(b)   Let A be an n element positive unimodal array. Design a $O(\log n)$-time sequential algorithm to find the maximum element of A.

(c)   Suppose you have a parallel system with p processors and unrestricted access to shared memory (for accessing array A), how quickly can you solve the problem in part (b)?

(d)   How would your answers to parts (b) and (c) change if A was negative unimodal?

(e)   How would your answers to parts (b) and (c) change if A was bimodal?

Some online games have a set of servers S such that a player can connect to any server. Say that a player is *satisfied* if he or she is connected to a server with delay at most Δ. You are given a set S of servers and a set P of players such that array $assign(j) = k$ means player p_j is connected to server s_k. You are also given a delay matrix D such that $D(j, k)$ is the delay between player p_j and server s_k. Each server has capacity c; a server is *full* if it has c players assigned to it.

When a player p_g leaves the game from a full server s_h, then we can try to increase the number of satisfied players by the following algorithm. For each unsatisfied player (player with delay $> \Delta$), check if its delay to s_h is at most Δ, and if so, move the player to server s_h. Quit this algorithm when either moving an unsatisfied player to s_h or after testing all unsatisfied players and discovering that no player will be satisfied by moving to s_h.

Attempt to improve this algorithm for increasing the number of satisfied players as follows.

(a) Describe an efficient data structure for each server s_h that holds the set of unsatisfied players that would be satisfied if they were assigned to s_h.

(b) Describe an efficient algorithm using these data structures to attempt to increase the number of satisfied players when player p_g leaves full server s_h.

(c) What is the time complexity of this algorithm? How much time does it take to update the data structures?

(d) Suppose a new player p_{new} joins the game but receives an unsatisfying assignment. Describe how to update the data structures from part (a) and how much time this takes.

A set of n stations share a channel that each processor could write to and read from. At any time the value read from the channel is the same for all stations and is called the *channel symbol*. For this problem, the channel symbol can take one of three values, $0, 1, \#$.

If no station writes to the channel, then the channel symbol is 0. If exactly one station writes to the channel then the channel symbol is 1; the value written by the station is not important. If more than one station writes to the channel, then the channel symbol is $\#$ (a special collision symbol).

This problem involves a MAC protocol, in which Q "active" stations (where $2 \leq Q \leq n$) wish to acquire the channel. The active stations participate in a competition to win the channel; while the value of Q is known to each active station, which other stations are active is is not known. At the end of the competition one active station is selected as leader and it acquires the channel. All other active stations are aware that they are not the leader. The stations select a leader using a randomized algorithm. The algorithm runs for several (potentially unbounded number of) rounds until a leader has been selected. The algorithm terminates once the leader has been selected. The following algorithm is executed in each round by each active station i that wishes to acquire the channel.

```
/* Executed in parallel by all active stations i */
    Station i flips a coin with probability 1/Q of heads and probability 1 − 1/Q of tails
    Station i writes to the channel if and only if it flips heads
    Station i reads from the channel
    if the channel symbol is a 1 then
        if Station i wrote to the channel in the current round then
            Station i terminates as leader
        else Station i terminates as non-leader
        end_if_else
    end_if
```

Answer the following questions. All answers must be justified.

(a)   Illustrate the algorithm for $Q = 2$ that terminates in 3 rounds, with channel symbols 0 and $\#$ in the first two rounds.

(b)   For the general case of Q stations wishing to acquire the channel, what is the probability that exactly one station will write to the channel?

(c)   You are given that $\left(1 - \frac{1}{x}\right)^{x-1} > e^{-1} \approx 0.368$. Show that, on an average, the above algorithm terminates in a constant number of rounds (independent of Q).

(d)   Indicate how you may approach the problem if each station did not know the value of Q.

Let $P = \{p_1, p_2, \ldots, p_n\}$ be a set of points in the plane. A *planar subdivision* of P is a graph $G = \{V, E\}$ embedded in the plane, where $V = P$ and each edge $e = (p_i, p_j) \in E, p_i, p_j \in P$ is a straight line segment. A *maximal planar subdivision* S of P is a planar subdivision such that no new edge connecting two vertices can be added to S without destroying its planarity, i.e., any edge that is not in S intersects one of the existing edges. A *triangulation* of P is a planar subdivision of P where each bounded facet is a triangle. The left figure is a planar subdivision, and the right figure is a triangulation.
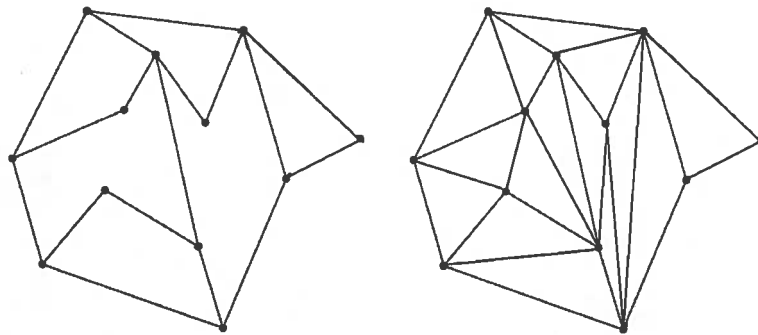
a) Prove that a maximal planar subdivision of P is a triangulation.

b) Is a triangulation always a maximal planar subdivision? If so, prove it; if not, give a counter example.

c) Consider a convex polygon with n vertices on its boundary, without introducing new interior point, one can construct a triangulation of this polygon. Does each triangulation scheme have the same number of triangles? If so, how many? If not, explain why.

d) Suppose an arbitrarily given polygon has n vertices on the boundary and m points inside the polygon; a triangulation that taking all these $n+m$ points as vertices can be constructed. Does each triangulation scheme have the same number of triangles? If so, how many? If not, explain and derive the number.

We have a setup consisting of (i) a point light source with radiance intensity I, located at (x_s, y_s, z_s), (ii) a mirror with size d-by-d, located in the xz-plane, and (iii) a planar surface of infinite size, located in the xy-plane.

Note that $x_s = 0$ and $z_s < d$.
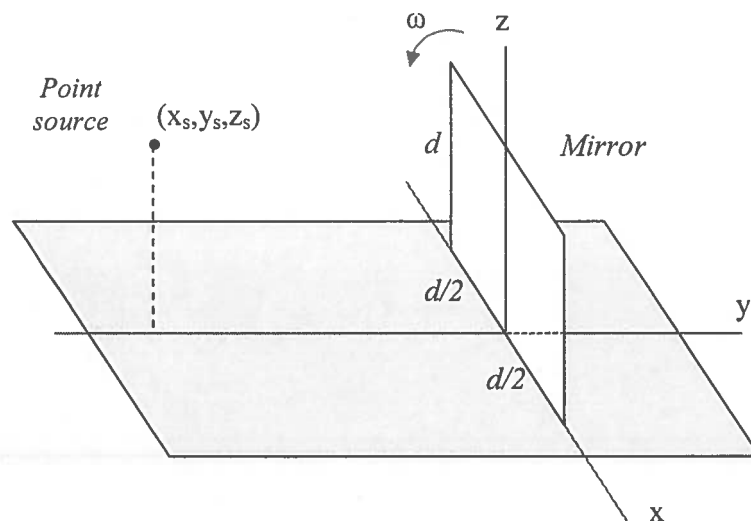
(a) What is the irradiance right below the point source?

(b) What is the irradiance at an arbitrary point on the surface?

(c) Suppose that the mirror starts to rotate along the x axis with an angular velocity of ω in the direction shown in the figure. Derive the irradiance right below the point source and plot it as a function of time.

(State any assumptions you make in your solutions.)

Quadric patches are 3D surfaces that can be represented implicitly as

$$S(x, y, z) = ax^2 + by^2 + cz^2 + dxy + eyz + fxz + gx + hy + jz + k = 0. \quad (1)$$

a) Many simple geometric primitives are in the family of quadric surfaces. Describe the coefficients of spheres, ellipsoids, cylinders, and planes.

b) Any quadric surface patch can be formulated using a matrix representation,
$$P^T Q P = 0,$$
where P is a 4×1 vector and Q is a 4×4 symmetric matrix. Derive P and Q from equation (1).

c) Given a 3D surface patch S, to compute its following geometric properties:

   (i) the normal of point $\mathbf{p}(x, y, z) \in S$ on the surface,

   (ii) whether a point $\mathbf{q}(x, y, z)$ is on S or not,

   (iii) hidden surface determination through z-buffering, namely, given the x and y coordinates of a point $\mathbf{p} \in M$ on the surface M, to check $\mathbf{p}$'s depth coordinate z,

which representation scheme, triangle mesh or implicit quadric representation described above, is more efficient? You should elaborate your comparison on each of these three computations.

Circuits and Systems
Problem 2

1) In the circuit below the delay line is a cable, whose length is initially short compared to the rise time of the transistor, which has a high β. What is the voltage at the base of the transistor?

2) The length of the cable is increased until its delay is 1 microsecond, which is long compared to the risetime of the transistor. What is the frequency at which the circuit oscillates?

3) What is the amplitude of oscillation, as measured at the collector of the transistor?

5 V

1 kΩ

100 Ohm delay line

1 kΩ
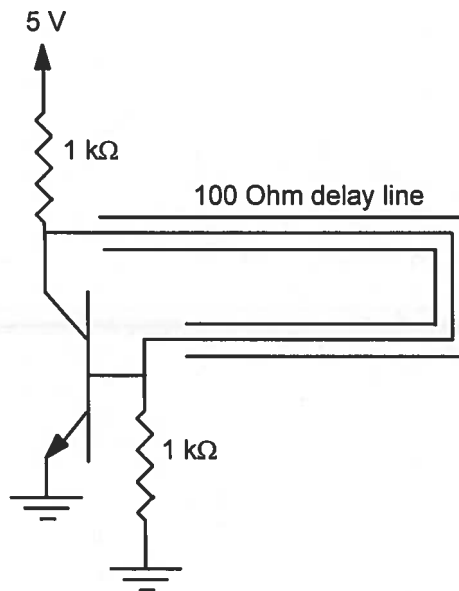
Circuits and Systems
Problem 3

Calculate the resistance of the following structures.

    a. Calculate the resistance of a rod with a diameter of 100 um and a length of 1 mm. The resistivity is ρ=0.5 ohm·cm (You can assume that π is equal to 3.)

    b. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).
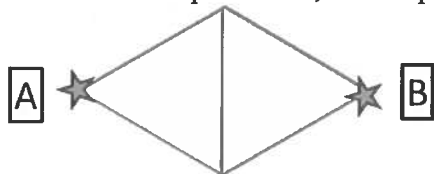
    c. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).
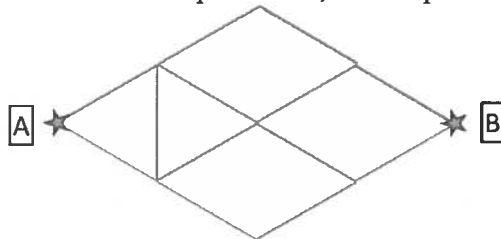
    d. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).
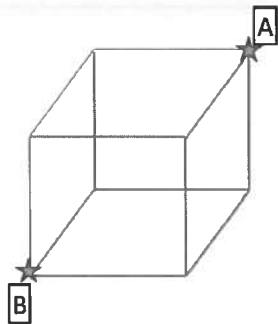
    e. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).
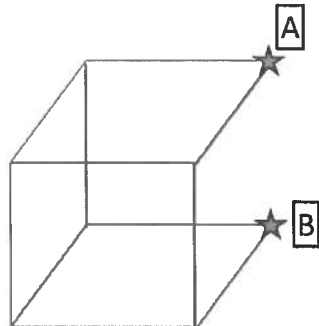
Physical Electronics
Problem 1

The energy E versus k relationship in a direct band gap compound semiconductor material (*material A*) for electrons in the valence band is given by $E = E_0 + A\cos ak$, where E_0, A and a are material constants and k is propagation constant (radians/m).

  a) Find the effective mass for valence band holes in this material at the top of the valence band i.e. band edge at $E = E_V$. Show intermediary steps.
  b) Current I = 1 mA flows through a bar made from p-type doped *material A* as shown in Fig. 1 below when $V_B = 5$ V.
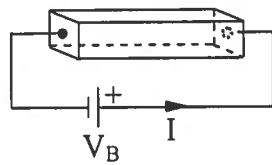

Fig. 1

The composition of the material is slightly changed so that in this new semiconductor (*material B*), the E versus k relationship for electrons in the valence band is now given by: $E = E_0 + 2A\cos ka$. What will be the value of current I for this case if the bar in Fig. 1 is replaced by a bar made from *material B* having an identical size, shape and doping density? You may assume all other material properties to remain the same for these two materials. You must explain your answer clearly. State any assumptions made.

  c) Now assume that for *material B*, the mean free time between collisions for holes (relaxation time) decreases to 0.8 times its value in material A. Repeat part b) above for this case (i.e. find the new value of I for this case). You must explain your answer clearly.

Physical Electronics
Problem 2

A silicon n-channel MOSFET has substrate doping $N_A = 10^{16}$ cm^{-3} and threshold voltage $V_T = 0.75$ V. The substrate is grounded. Both drain and source regions are heavily doped. Temperature $T = 300$ K.

   a) Draw the cross-section of the MOSFET at the on-set of saturation showing all regions of the device. Carefully label your figure.
   b) Determine the minimum channel length L (μm) so that the incremental change ΔL is no more than 0.1L (10 % of L) when drain to source voltage $V_{DS} = 5$ V and gate to source voltage $V_{GS} = 5$ V. Show intermediary steps and state any assumptions made. Explain your approach.
   c) Will the value of L be smaller or larger or same compared to the case a) above if now $V_{GS} = 2$V keeping V_{DS} constant at 5 V? Explain your answer giving reasons.

Depletion width W in a p-n junction is given by: $W = \sqrt{\dfrac{2\varepsilon_s}{q}\left(\dfrac{1}{N_A}+\dfrac{1}{N_D}\right)(V_{0bi}-V)}$ where

permittivity of Si $\varepsilon_s = 11.7\ \varepsilon_0$, permittivity of free space $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, magnitude of electron charge $q = 1.6 \times 10^{-19}$ C, V_{0bi} is built in junction voltage and V is forward bias voltage applied to a diode. Boltzmann constant $k = 8.62 \times 10^{-5}$ eV/K, temperature $T = 300$ K, intrinsic carrier density in Si $n_i = 1.5 \times 10^{10}$ cm^{-3} at 300 K, and Si band gap is 1.12 eV.

Physical Electronics
Problem 3

The lattice structure of a crystal is body-centered cubic (bcc). However, the Bravais lattice of this same crystal is a simple cubic (sc) structure.

a) For incident X-rays of wavelength (λ) equal to 1.542 Å, find the Bragg angles of X-rays scattered from the Bravais lattice of this crystal.

b) Find the primitive vectors ($\mathbf{b}_1$, $\mathbf{b}_2$, $\mathbf{b}_3$) of the reciprocal lattice for the sc lattice structure. The reciprocal lattice formula is as follows:

$$\mathbf{b}_1 = 2\pi \frac{\mathbf{a}_2 \times \mathbf{a}_3}{\mathbf{a}_1 \bullet (\mathbf{a}_2 \times \mathbf{a}_3)}$$

$$\mathbf{b}_2 = 2\pi \frac{\mathbf{a}_3 \times \mathbf{a}_1}{\mathbf{a}_1 \bullet (\mathbf{a}_2 \times \mathbf{a}_3)}$$

$$\mathbf{b}_3 = 2\pi \frac{\mathbf{a}_1 \times \mathbf{a}_2}{\mathbf{a}_1 \bullet (\mathbf{a}_2 \times \mathbf{a}_3)}$$

-where $\mathbf{b}_1$, $\mathbf{b}_2$, and $\mathbf{b}_3$ are the reciprocal lattice vectors corresponding to direct lattice vectors $\mathbf{a}_1$, $\mathbf{a}_2$, and $\mathbf{a}_3$.

c) Repeat part b) for the bcc lattice structure.

Physical Electronics
Problem 4

A coaxial capacitor consists of two conducting coaxial surfaces of radii a and b ($a<b$). The space between is filled with a dielectric material with dielectric constant ε_r.

(a) Use Gauss's law to calculate the capacitance per unit length.

(b) If the space between the two conducting surfaces is filled with two different dielectric materials with dielectric constants ε_{r_1} for $0<\phi<\pi$, and ε_{r_2} for $\pi<\phi<2\pi$ (see figure below), calculate the capacitance per unit length in two different ways:

i) Using Gauss's law.

ii) Using the fact that this configuration can be seen as two capacitors in parallel.

(c) Assuming that $b=3a=1.5$ cm , $\varepsilon_{r_1}=2.3$, $\varepsilon_{r_2}=5.4$, calculate the capacitance per unit length. (The free space permittivity is $\varepsilon_0=8.854\times10^{-12}$ F/m .)
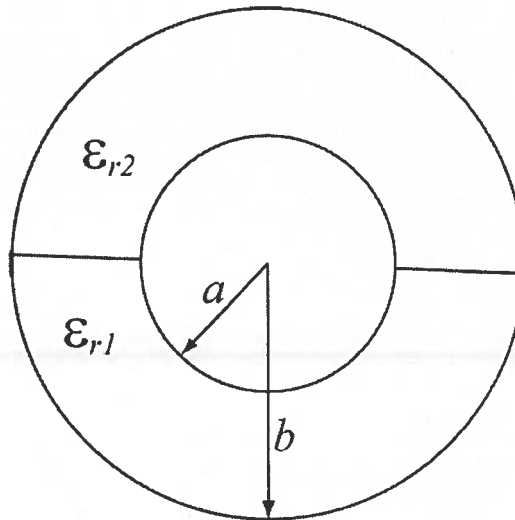
Physical Electronics
Problem 5

Consider a plane wave in free space with electric field $\mathbf{E}_i = \hat{x}E_0 \exp(-j\beta_0 z)$ ($\beta_0 = \omega\sqrt{\varepsilon_0\mu_0}$), which is normally incident on a dielectric slab of length d and dielectric constant $\varepsilon = \varepsilon_r\varepsilon_0$ ($\varepsilon_r > 1$). The slab is bounded from a perfect electric conductor (PEC), which occupies the $z>d$ half-space. The electric field of the reflected wave for $z<0$ is $\mathbf{E}_r = \hat{x}RE_0 \exp(j\beta_0 z)$, where R is the reflection coefficient. All fields have harmonic time dependence $\exp(j\omega t)$.

(a) Find the amplitude of the reflection coefficient $|R|$.

(b) Find the reflection coefficient R when $\beta d = \pi$, where $\beta = \omega\sqrt{\varepsilon\mu_0}$.

(c) Find the reflection coefficient R when $\beta d = \dfrac{\pi}{2}$.

(d) Find the surface current density at the interface between the slab and the PEC when $\beta d = \pi$.


$\mathbf{E}_i$ ε_0 Incident wave ε d PEC $z=0$ $z=d$ X   Z
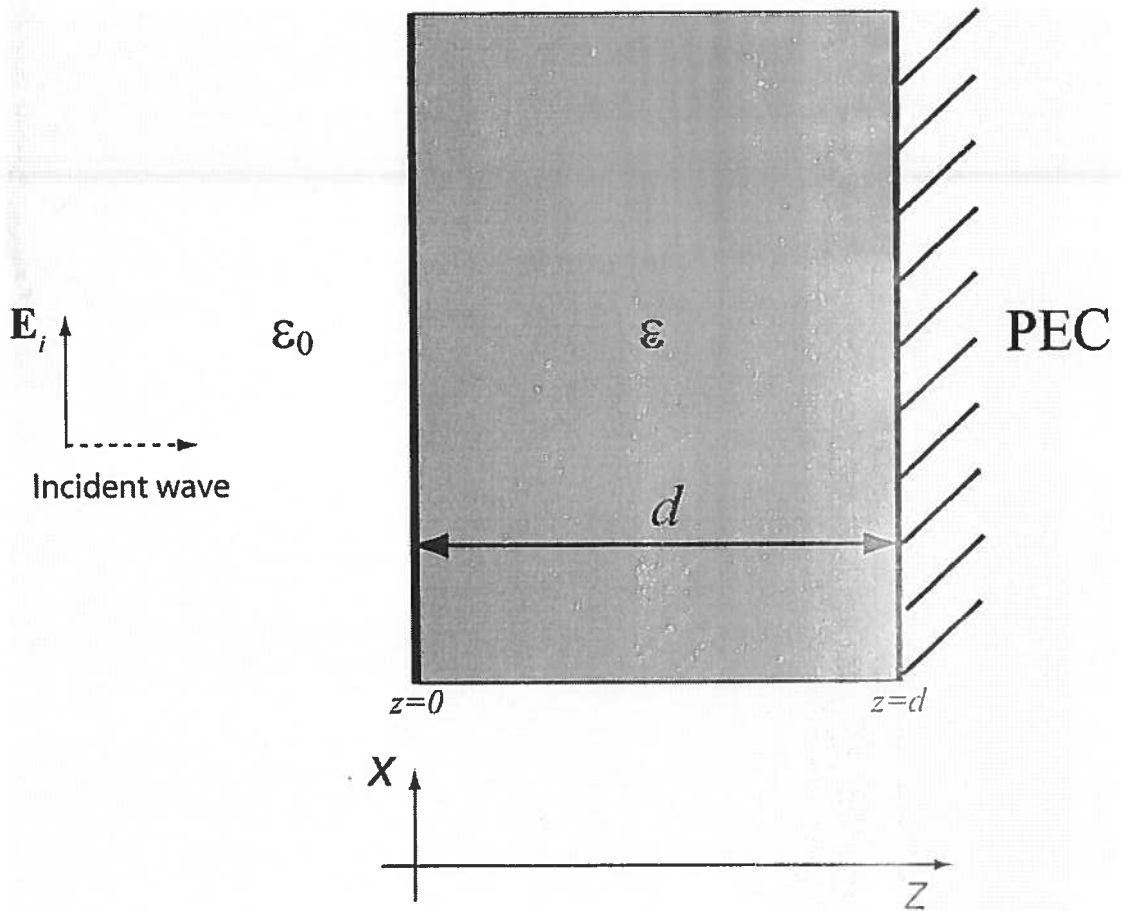
Physical Electronics
Problem 1

A silicon diode has the doping profile as shown in the figure below. N_D and N_A are donor concentration and acceptor concentration, respectively. Given,

$$p_0 = n_i \exp\left(\frac{E_i - E_F}{kT}\right) \quad \text{and} \quad n_0 = n_i \exp\left(\frac{E_F - E_i}{kT}\right)$$

where n_i is the intrinsic carrier concentration, E_i is the intrinsic Fermi level, E_F is the Fermi level, k is the Boltzmann constant and T is the temperature. n_0 and p_0 are electron and hole concentrations in equilibrium. x_n and x_p are n-side and p-side widths of the depletion region. Assume that $-x_p < -x_0$ for all applied biases of interest.
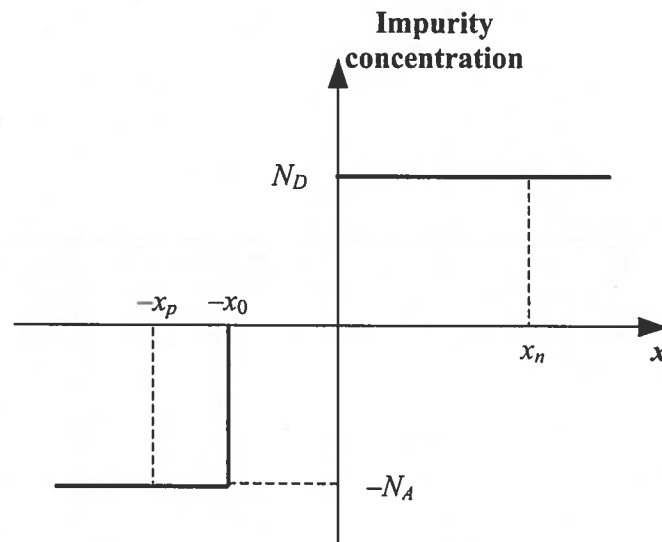

Given, $n_i = 1.45 \times 10^{10}$ cm^{-3}, $k = 1.38 \times 10^{-23}$ J/K, $T = 300$ K, $N_D = 5 \times 10^{15}$ cm^{-3}, $N_A = 1 \times 10^{16}$ cm^{-3}, and $x_0 = 0.5$ μm.

(a) Assuming impurities are 100% ionized, derive the expression for the built-in potential at thermal equilibrium. Justify your answer and show detailed steps.

(b) Calculate the built-in voltage (V_{bi}), x_n, and x_p.

(c) Draw an equilibrium band diagram.

(d) When a forward bias of 0.45 V is applied, repeat (b).

Physical Electronics
Problem 3

The figure below illustrates a semiconductor block for measuring the Hall effect. A current (I) is applied in $+y$ direction and a magnetic field (B) is applied in $+z$ direction. Answer the following questions.
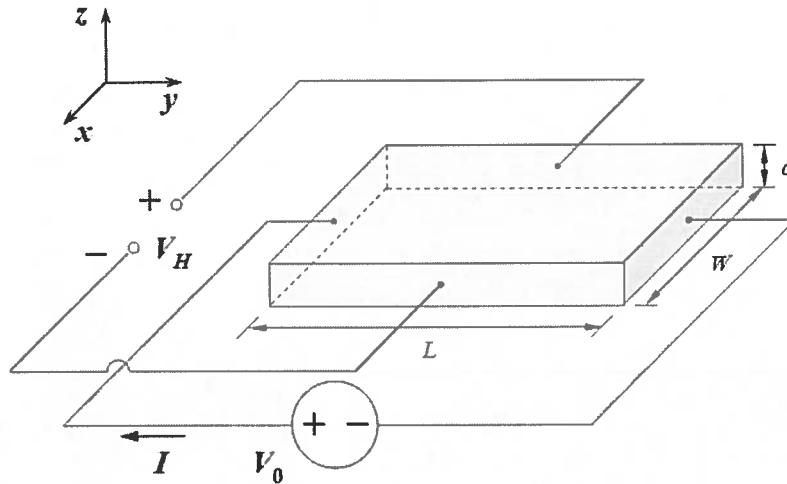

(a) Explain how the Hall effect can be used to distinguish the doping type of a semiconductor.

(b) Derive an expression of the Hall voltage V_H for a p-type semiconductor. Define parameters if necessary.

(c) Consider that the silicon Hall sensor whose geometry is $L = 1$ mm, $W = 50$ μm, and $d = 5$ μm in the figure shown above is placed in the known magnetic field (B). When $B = 50$ mT (or 0.05 Wb/m^2), $I = 1$ mA, and $V_0 = 5$ V, the measured Hall voltage (V_H) is 5 mV. Determine the type, concentration, and mobility of the majority carrier.

(d) Will the Hall voltage have temperature dependence? Present your view on this.

1. The synchronous generator has the terminal voltage of 4 kV and it should be connected to the power line of 2 kV. What should be done to enable the generator to be connected to this line?
2. The nominal frequency of 3-phase synchronous generator is 50 Hz. What should be done in order to connect this generator to 3-phase system of the same nominal voltage but of 60 Hz frequency?
3. The electric energy should be send through the transmission line with the lowest power losses. What would you do to achieve this goal?
4. The induced phase voltage of 3-phase synchronous generator is distorted from sinusoidal shape and it contains the 3-d harmonic. The generator is connected to a 3-phase load. What would you do to make the 3-d harmonic of the current not to flow?

A. Develop power equation of the three-phase unbalanced linear-time invariant (LTI) load specified in terms of line-to-line admittances for harmonics Y_{RS}, Y_{ST}, Y_{TR}, assuming that the supply voltage is sinusoidal, but symmetrical and of the positive sequence.

B. Specify phenomena that affect the power factor of such loads.

C. Calculate the rms values of the active, reactive and unbalanced currents in the circuit shown in Figure and the power factor, λ, of the supply, assuming that $Z_R = 2+j3$ Ω.
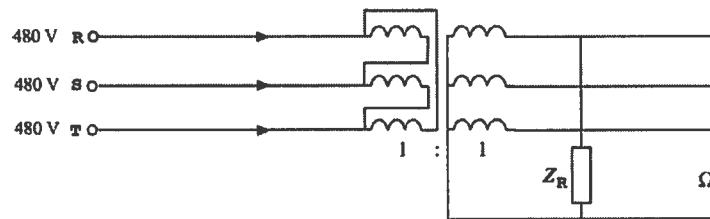
A Buck-Boost DC/DC converter supplied with voltage $U = 200$ V is used for the control of the output voltage on the resistance $R_0 = 15 \ \Omega$ from $U_1 = 100$ V to $U_2 = 300$ V. Draw the structure of the converter, the waveforms of the inductor and capacitor currents. Calculate inductance L and capacitance C of the converter if the switching frequency is equal to $f = 15$ kHz and output voltage ripples cannot be higher than 5 % of the output voltage.

1. Draw the equivalent circuit of a single-phase transformer. What kind of measurements have to be done to determine the parameters of this circuit?
2. Draw the phasor diagrams of currents and voltages, one for the inductive and one for pure resistive load. Show when the voltage regulation is greater.
3. A single phase transformer built (in Europe) for the rated frequency of 50 Hz is going to be connected to the power line (in US) of rated voltage and 60 Hz frequency. Will the power losses in the transformer increase or decrease with respect to those at 50 Hz frequency (assuming the transformer is loaded by the rated current in both circumstances). Explain what kind of power losses and why.
4. 3 single-phase transformers of the turn ratio 10:5 are connected to the 3 phase line of 220 V line voltage. Their primary and secondary windings are connected, first both in Δ and next both in Y.
    *   Draw the circuit diagrams for both cases
    *   What are the secondary phase voltage and the line voltage in each of the two connections?

1. Draw the equivalent circuit of the very long high voltage transmission lines. Draw its simplified equivalent circuit with a resistance, inductance, and capacitance.
2. Is there any limit of power transmitted by the line? Which of the line, resistive or inductive can transmit more maximum power?
3. How to minimize the voltage regulation (caused by the voltage drop along the transmission line) of the receiver? Is it possible to minimize it to zero? Explain how.
4. Draw the equivalent circuit of the inductive transmission line linking two systems. Using the voltage phasor diagram explain when the power can be transmitted from one system to another if the magnitudes of the voltages of both systems are equal.

Design a micro grid of PV rated at 200KW of power and at 230 V AC using a PV module with the following voltage and current characteristics. Determine the following:

    a. Number of modules in a string for PV type 1
    b. Number of strings in an array for PV type 1
    c. Number of arrays
    d. Inverter specifications
    e. One-line diagram of the system

TABLE 5.47 Photovoltaic Module Data.

Panel	Type 1	Type 2	Type 3	Type 4
Power (Max). W	190	200	170	87
Voltage at max. power point (MPP), V	54.8	26.3	28.7	17.4
Current at MPP, A	3.47	7.6	5.93	5.02
V_{OC} (open-circuit voltage), V	67.5	32.9	35.8	21.7
I_{SC} (short-circuit current, A	3.75	8.1	6.62	5.34
Efficiency	16.40%	13.10%	16.80%	>16%
Cost	$870.00	$695.00	$550.00	$397.00
Width	34.6"	38.6"	38.3"	25.7"
Length	51.9"	58.5"	63.8"	39.6"
Thickness	1.8"	1.4"	1.56"	2.3"
Weight	33.07 lbs	39 lbs	40.7 lbs	18.3 lbs

1- What is the maximum power transferable to the load? (Assume a constant power factor – i.e. P/Q=constant and neglect R)

2- Draw a typical graph of load voltage vs. active power

3- Explain at least one method to overcome the voltage drop in case of high active power drop.
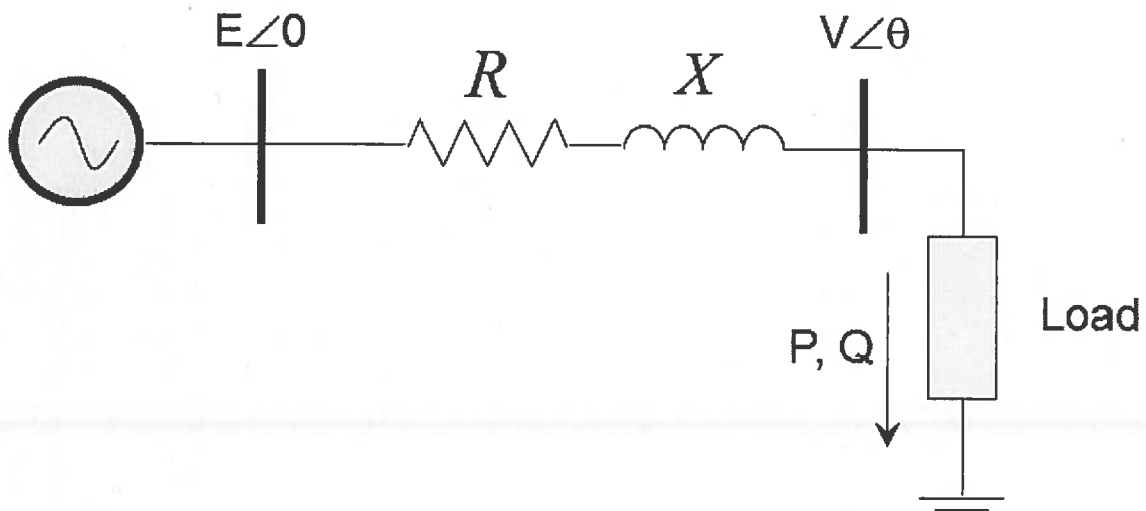
Consider open-loop transfer functions

$$L_1(s) = \frac{K(s-5)}{(s+5)(s^2+5s+6)}, \quad L_2(s) = \frac{K(s+1)}{s^2(s+2)}.$$

(i) Sketch Bode diagram for $L_1(s)$ and Nyquist plot for $L_2(s)$.

(ii) Determine the stability range of K for the closed-loop system with open-loop transfer function $L_1(s)$.

(iii) Determine the stability range of K for the closed-loop system with open-loop transfer function $L_2(s)$.

Consider a linear system

$$\dot{x} = Ax + Bu, \quad y = Cx$$

with

$$A = \begin{bmatrix} A_1 & 0 \\ 0 & A_2 \end{bmatrix} \quad B = \begin{bmatrix} B_1 & 0 \\ B_3 & B_2 \end{bmatrix} \quad C = \begin{bmatrix} C_1 & C_2 \end{bmatrix}$$

(i) Give at least two methods for checking the controllability and observability for this system.

(ii) If (A_i, B_i) are controllable for $i = 1, 2$. Is (A, B) controllable? If it is, prove your conclusion using one of the methods you have described in the part (i). If it is not, give a counter example.

(ii) If (A_i, C_i) are observable for $i = 1, 2$. Is (A, C) observable? If it is, prove your conclusion using one of the methods you have described in the part (i). If it is not, give a counter example.

Verify if any of the following statements are correct. If yes, give a proof or justification. If not, give a counterexample or a proof.

1. $\dot{x} = Ax + bu_1$ is controllable if and only if $\dot{x} = Ax + bu_1 + Abu_2$ is controllable.

2. $\dot{x} = Ax + bu$ is controllable if $\dot{x} = Ax + Abu$ is controllable.

3. If A is stable, then $\dot{x} = Ax + bu$ is controllable if and only if $\dot{x} = Ax + Abu$ is controllable.

4. If A is stable, then $\dot{x} = Ax + bu$ is controllable.

Consider a unity negative feedback with an open loop transfer function

$$G(s) = \frac{20}{(s+1)(s+10)}$$

Design a controller so that steady state error respect to a unit ramp input is no more than 0.1 and settling time is no more than 1 second.

Let $G(s)$ be a transfer matrix

$$G(s) = \begin{bmatrix} \frac{1}{s(s+2)} & \frac{1}{s} \\ \frac{10}{s+2} & \frac{s}{s+1} \end{bmatrix}$$

(i) Find a minimal state space realizaiton.

(ii) Based on the state space realization in (i), find a state feedback control law so that the closed-loop poles are in $\{-1, -2, -3\}$.

(iii) Find a state observer so that the observer poles are at $\{-10, -10, -10\}$.

(iii) Find all transmission zeros of the transfer matrix.

Sketch root locus for

(i) $G(s) = \dfrac{s+2}{s(s+1)(s+3)(s+4)}$ (ii) $G(s) = \dfrac{s+4}{s(s+1)(s+2)(s+3)}$

and indicate the centroid, asymptotes, and $j\omega$-axis crossover frequency, if there is one.

Let A be a real square matrix of dimension $n \times n$, B of dimension $n \times 1$, and C of dimension $1 \times n$. Consider the following Lyapunov equation:

$$AX + XA + BC = 0.$$

Assume that $\lambda_i(A) + \bar{\lambda}_k(A) \neq 0$ for all (i, k). Show that the solution X is nonsingular, if and only if (A, B) is controllable and (C, A) is observable.

Consider the following discrete-time linear and time-invariant (LTI) system

$$y[n] + y[n-1] - 12y[n-2] = x[n],$$

where $x[n]$ and $y[n]$ are, respectively, the input and output sequences.

1. Determine the frequency response of the above LTI system.

2. Determine the total solution for $n \geq 0$ of the above LTI system for an input $x[n] = 5\mu[n]$ and with the initial conditions $y[-1] = -1$ and $y[-2] = 1$. Here, $\mu[n] = 1$ for $n \geq 0$ and 0 for $n < 0$.

The impulse responses of two discrete-time linear-time-invariant systems (filters) are given by $h[n]$, $g[n]$; their z-transforms are given by $H(z)$ and $G(z)$, respectively. Note that $h[n]$ and $g[n]$ can be *finite-impulse-response* (FIR) or *infinite-impulse-response* (IIR) systems. Also note that the frequency response of a lowpass filter is nonzero at zero digital frequency; the frequency response of a highpass filter is nonzero at the digital frequency of $\pm\pi$.

1. Suppose $h[n]$ is an FIR filter with filter length $N + 1$, i.e., $h[n] = 0$, for $n < 0$ and $n > N$, where N is an arbitrary positive integer. If $h[n] = -h[N - n]$, for all n, show that $h[n]$ is never a lowpass filter.

2. Suppose $g[n]$ is an FIR filter with filter length $N+1$, i.e., $g[n] = 0$, for $n < 0$ and $n > N$, where N is an arbitrary positive integer. If $g[n] = g[N - n]$, for all n, show that $g[n]$ is never a highpass filter.

3. If $G(z) = H(-z^{-1})$, determine $g[n]$ in terms of $h[n]$. If $H(z)$ is a highpass filter, show that $G(z)$ is a lowpass filter .

4. A lowpass filter $h[n]$ is an FIR filter with filter length $N + 1$, i.e., $h[n] = 0$, for $n < 0$ and $n > N$, where N is an arbitrary positive integer. Assume that $G(z) = z^{-N}H(z^{-1})$. Determine $g[n]$ in terms of $h[n]$. Is $G(z)$ lowpass or highpass?

The unit-step input signal $u(n)$ is defined as 1 for $n \geq 0$ and 0 for $n < 0$. Consider a causal, linear and time-invariant (LTI) system whose input signal is given by $x(n) = u(n-1)$ and whose output signal is given by

$$y(n) = 2u(n) - (0.5)^n u(n).$$

1. Determine the impulse response $h(n)$ of this LTI system for all n and justify all steps.

2. Determine whether the LTI system is memoryless or not.

3. Determine whether the LTI system is stable or not.

4. If the LTI system has the input signal $x(n) = (0.5)^n u(n) + u(-n)$, determine the corresponding output signal $y(n)$.

Assume that $\{X_n\}$ is a zero-mean, wide-sense stationary random sequence with autocorrelation function $R_X[k] = E[X_n X_{n+k}]$. The random sequence $\{Y_n\}$ is obtained from $\{X_n\}$ by $Y_n = \alpha^n X_n + X_{n-1}$, where α is a real-valued constant.

1. Find the autocorrelation function of $\{Y_n\}$.

2. Find the cross-correlation function of $\{X_n\}$ and $\{Y_n\}$.

3. Determine those values of α for which $\{Y_n\}$ is wide-sense stationary.

4. Determine those values of α for which $\{X_n\}$ and $\{Y_n\}$ are jointly wide-sense stationary.

A digital communication system with two equiprobable messages uses the following signals

$$s_1(t) = \begin{cases} 2 & 1 \leq t \leq 2 \\ 0 & \text{else} \end{cases}$$

$$s_2(t) = \begin{cases} -2 & 1 \leq t \leq 2 \\ 0 & \text{else} \end{cases}$$

1. Assume that the channel is additive white Gaussian noise (AWGN) with noise power spectral density of $N_0/2$. Determine the error probability of the optimal receiver.

2. Assume a two-path channel as shown in the following figure where $A = 1$. The noise processes $\{N_1(t)\}$ and $\{N_2(t)\}$ are independent white Gaussian noise processes each with power spectral density of $N_0/2$. The receiver receives both $r_1(t)$ and $r_2(t)$ and makes its decision regarding the message based on this observation. Find the structure of the optimal receiver and calculate its error probability.

3. Now suppose A is a random variable which is uniformly distributed on the interval $[0, 1]$ and is independent of the message sequence and the noise process.. When message m is transmitted, $r_2(t) = as_m(t) + N_2(t)$ is received where a is the outcome of A. Suppose that the receiver knows the value of a.

   (a) What is the structure of the receiver in this case?

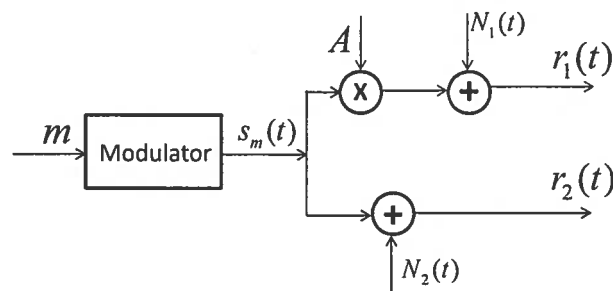   (b) Find the the average error probability of the receiver.

Figure 1:

In Figures 2 are two block diagrams illustrating the modulation and demodulation processes without directly using a sinusoidal signal $\cos(\omega_0 t)$.

Filters with impulse responses $h(t)$ and $g(t)$ are used at transmitter and receiver to produce $m(t)\cos(\omega_0 t)$, and $m(t)$, respectively. Here, $m(t)$ is the desired message signal whose bandwidth is B, i.e., its Fourier transform $M(j\omega) = 0$ for $|\omega| > B$, and $\omega_0 > 2B$ is the carrier frequency (See Figure 3).

The periodic signal $x(t)$ shown in Figure 3 has fundamental period $T_0 = \frac{2\pi}{\omega_0}$. In order to restore $m(t)$ at the output of $g(t)$, the following questions should be addressed in a sequel.

1. Compute the Fourier series $\{a_n, n = \cdots - 1, 0, 1, \cdots\}$, and Fourier transform of $x(t)$.

2. Determine the frequency response of the filter $h(t)$ so that its output is given by $r(t) = m(t)\cos(\omega_0 t)$.

3. Determine and draw the Fourier transform $Z(j\omega)$ of $z(t) = r(t)x(t)$.

4. Determine the Fourier transform $G(j\omega)$ of $g(t)$ to exactly restore $m(t)$ at the output of $g(t)$.
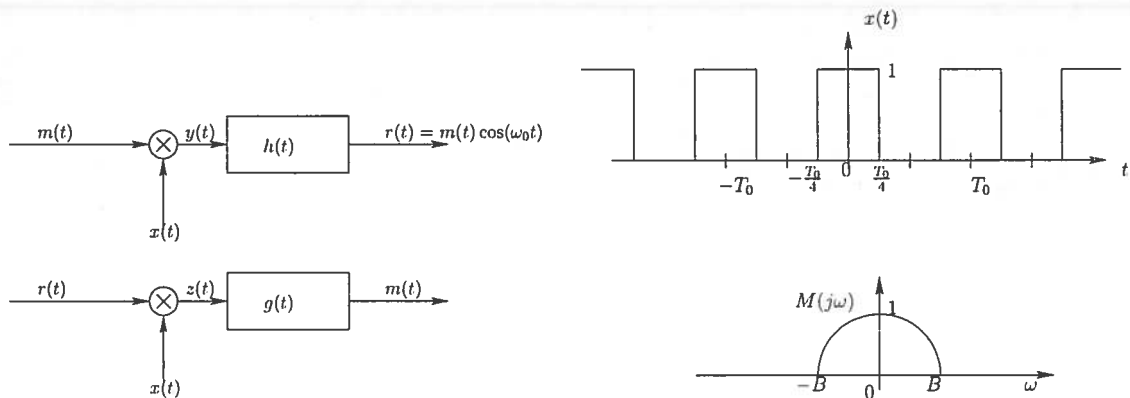
(a) Figure 2: Transmitter and Receiver Block Diagrams
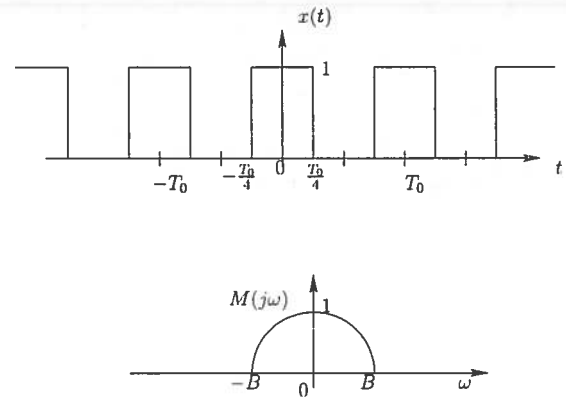
(b) Figure 3: Periodic Signal $x(t)$ and Fourier Transform $M(j\omega)$ of $m(t)$

The token bucket (TB) algorithm is used to shape the incoming traffic in a network and is different from the leaky bucket algorithm. Typically, the token bucket throws away tokens when the bucket is full but never discards packets, while the leaky bucket discards packets when the bucket is full. Figure 1 illustrates the basic principle of the token bucket. Note that the TB accumulates fixed size tokens in a token bucket. It then transmits a packet (from the data buffer), if any, or an arriving packet if the sum of the token sizes in the bucket add up to packet size. More tokens are periodically added to the bucket. Tokens to be added when the bucket is full are discarded. From Figure 1, if C bytes is the maximum capacity of a bucket, R bytes/sec is the token arrival rate, and M bytes/sec is the maximum output rate, then the Burst Length in S sec can be calculated as C + RS = MS

Rate R bytes/sec
Token generator

Token buffer
Capacity C
bytes

Cell or packet

Data buffer
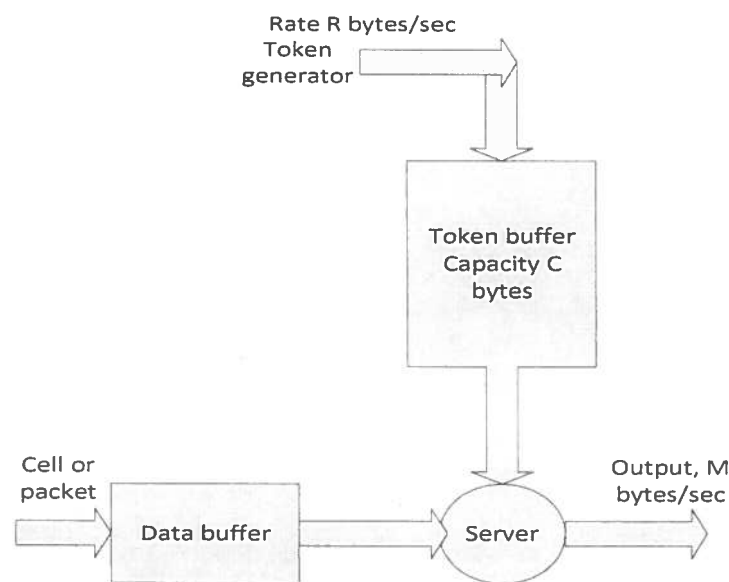
Server

Output, M bytes/sec

Figure 1: Token bucket for traffic shaping

Consider three flows of traffic that merge at a point in the network just before going through a token bucket policer, which drops all non-conforming packets. Assume that all packets are of the same size and that each token corresponds to a permission to transmit exactly one packet. Flow 1 generates a packet at periodic intervals of two seconds, at time instants $t = 0$, $t = 2$, $t = 4$ and so on. Flow 2 generates a packet at periodic intervals of three seconds, at time instants $t = 1$, $t = 4$, $t = 7$ and so on. Flow 3 generates a packet at periodic intervals of six seconds, at time instants $t = 2$, $t = 8$, $t = 14$ and so on. Assume that packet transmission times are negligible. Assume that the bucket is full of tokens before the first packet arrives at time $t = 0$ and that the next new token is generated at time instant $t = 0.25$.

(a) What is the minimum necessary token generation rate R such that no tokens are ever dropped?

(b) Given the minimum necessary token generation rate, what is the minimum necessary size of the token bucket so that no packets are ever dropped? Prove your answer.

This problem is regarding to program co-scheduling on chip-multiprocessors (CMPs). In CMPs, it is common for several cores to share the last level cache. This sharing brings cache contention between co-running jobs. Therefore, a clever job co-scheduling is very important to achieve high performance for CMPs. Answer the following questions where a K-core CMP with a shared last level cache exists.

A. There are four programs which are required to be co-scheduled on a dual-core CMP (i.e., $K=2$). All the programs' execution time without resource contention are the same. The co-run performance degradations are listed in the following table. A co-run degradation is an increase in the execution time of an application when it shares a cache with a co-runner, relative to running solo. The value on the intersection of row i and column j indicates the performance degradation that application i experiences when co-scheduled with application j.

	W	X	Y	Z
W	-	40%	20%	3%
X	25%	-	1%	1%
Y	3%	5%	-	0.5%
Z	2%	3%	0.5%	-

   Now based on the above table, find out the best schedule and the worst schedule. The best schedule means that the overall execution time for all programs is minimal.

B. Figure out a polynomial time algorithm for a dual-core (i.e., $K=2$) scheduling for N jobs and compute its time complexity.

A hardware device needs to maintain a count of events for each of a large number of *locations*. Normally this would be done with a memory with L elements (storage locations) of w bits each, where $2^w - 1$ is the maximum event count. The device has a reset input which causes all memory elements to be set to zero.

The device needs to perform two operations. In an `increment(c)` operation element c of the memory is to be incremented. In a `compare(c,d)` operation the device is to set its `gt` output to `true` if the count in the memory at c is higher than the count at d (and `false` otherwise).

The goal of this problem is to analyze lower-cost versions of this device in which fewer than w bits would be stored per memory location, resulting in some `compare` operations returning the wrong value. Consider the following two cost reduction methods. Both use memory devices with L locations of $b < w$ bits each.

In Method 1 the `increment(c)` operation will obtain a random number and will only increment location c if the number is above some threshold.

In Method 2, the `increment(c)` operation will examine the retrieved value. If it is already at its maximum then all values in the memory will be *desaturated* by dividing each one by 2 (shifting right by one bit). After the desaturation, element c will be incremented.

(a) Which method is more likely to make errors on the `compare` operation? Provide examples to illustrate the errors. Quantify the error probability as best as possible using an assumed model of the values of `c` in a sequence of increment operations.

(b) Suggest improvements to desaturation that would reduce the error rate.

Single-event upsets from particle strikes have become a key challenge in processor design. The shrinking processor feature size, lower threshold voltage and increasing clock frequency make modern processors highly vulnerable to transient faults. Architectural Vulnerability Factor (AVF) reflects the possibility that a transient fault eventually causes a visible error in the program output, and it indicates a system's susceptibility to transient faults. To estimate the AVF, architects track the subset of processor state bits required for architecturally correct execution (ACE). Any fault in a storage cell that contains one of these bits, which we call ACE bits, will cause a visible error in the final output of a program in the absence of error correction techniques. We call the remaining processor state bits un-ACE bits, as their specific values are unnecessary for architecturally correct execution. A fault that affects only un-ACE bits will not cause an error. The AVF of a hardware structure is defined as follows.

$$AVF = \frac{\sum \text{residency (in cycles) of all ACE bits in a structure}}{\text{total number of bits in the hardware structure} \times \text{total execution cycles}}$$

A. In a 32-bit out-of-order pipelined processor whose instruction format list as follows. Rd is the destination register while Rs and Rt are two source registers. In case that only one source register is used, the Rt field remains as all "0".

Opcode (17 bits)	Rd (5 bits)	Rs (5 bits)	Rt (5 bits)

According to the above definition, what's the AVF for the following components or instructions: (1) branch predictor; (2) the program counter register for a committed instruction; (3) mispredicted instructions; (4) NOP instructions; (5) Dynamically dead instructions whose destination registers are not used any more. (6) Empty reorder buffer entries. Justify your answer.

B. In the processor described as part (A), the ROB has 6 entries with each has 70 bits which include the encoding bits of instructions and other bits such as program counter, status of the instruction (issued, completed, etc). The following program has been loaded into the ROB at the beginning of cycle 0.

```
        SUBUI       R3, R1, #2
        BNE         R3, L1
        ADDUI       R1, R0, #3
L1:     SUBUI       R3, R2, #2
        SUBUI       R1, R2, #5
        ADDI        R4, R4, #1
        ADD         R3, R1, R0
```

Right after cycle 2, the BNE instruction was found mispredicted. Therefore, the ADDUI instruction was squeezed. Then the program only has five instructions remain in the ROB. This means that there is an empty ROB entry starting from this point. All instructions finish and are flushed at the end of cycle 20. Calculate the AVF of ROB of this program. Justify your answer.

Appearing below are four MIPS assembly language versions of the following loop: `for ( int i=0;` `i<limit; i++ ) do_stuff(a[i]);`. The first one, Baseline, is straightforward. In the second one, Unrolled Offset, the loop has been unrolled by degree 4 (the unrolled loop body contains 4 copies of the original loop body, and the loop iterates for $\frac{1}{4}$ the number of iterations). The load instructions use offsets to avoid some memory address calculations. The last version, Unrolled pre-increment, uses a hypothetical MIPS pre-increment instruction to avoid incrementing r2 at the end of the loop.

```
LOOP: // Baseline
 lw r1, 0(r2)      // r1 = Mem[r2+0]; (Load 4-byte word from mem addr r2)
 // Do stuff.
 addi r2, r2, 4
 bneq r2, r4 LOOP  // If r2 != r4 goto LOOP.
 nop


LOOP4o:  // Unrolled Offset
 lw r1,  0(r2)
 lw r11, 4(r2)   // r11 = Mem[r2+4];
 lw r21, 8(r2)
 lw r31, c(r2)
 // Do stuff.
 addi r2, r2, 16
 bneq r2, r4 LOOP4o
 nop


LOOP4i:  // Unrolled Preincrement
 lw r1,  (r2+)
 lw r11, (r2+)   // r11 = Mem[r2];  r2 = r2 + 4;
 lw r21, (r2+)
 lw r30, (r2+)
 // Do stuff.
 bneq r2, r4 LOOP4i
 nop
```

(*a*) Suppose the do-stuff region in Baseline contained five instructions. By how much would the Unrolled Offset code improve performance over the Baseline code assuming **perfect execution** on an ordinary scalar (not superscalar) five-stage pipeline? Briefly explain your reasoning.

(*b*) The Unrolled Preincrement code uses a pre-increment load instruction, something not really present in MIPS. This instruction loads from memory at the address in r2 and then increments r2 by 4. Notice that the Preincrement code uses one less instruction than the Unrolled Offset code because it doesn't need an `add` instruction to increment r2.

      Consider a four-way superscalar statically scheduled MIPS implementation that has four of each unit, including four ALUs and four memory ports. The implementation has a full set of bypass paths. This ordinary four-way superscalar processor would have trouble executing one of the loops at full speed. Identify which loop would cause problems and explain why. Explain what an aggressive four-way processor could do to overcome the problems. (The problem is with the load instructions.)

(*c*) Propose an alternative to the offset and preincrement load instructions that would be inexpensive to implement and would run efficiently (fast and using little energy) with the unrolled code above.

In an out-of-order executed processor, a load instruction may obtain its address and value before a preceding (in program order) store instruction's address generation. In this case, if the processor executed the load instruction without any consideration about the early store instruction, program correctness would be violated if both instructions had true data dependence. Usually, we have two policies: (A) a conservative solution is stalling the load and its dependent instructions until the early store's address generation; (B) another alternative is predicting the memory dependence between loads and preceding stores. Memory dependence prediction allows some loads to bypass early stores if no dependence predicted. Otherwise, if dependence predicted, load values can be forwarded from the latest early stores without cache access. At the commit stage of stores, the processor check correctness of predictions, if not, loads and their dependent instructions would be re-executed.

Now consider a two-issue, out-of-order execution pipeline with following stages: Instruction Fetch (IF), Decode (ID), Issue (IS), Execution / Address Generation (EX), Write Result (WR), Commit (CT). There are two integer ALU units, two load/store units and one MUL unit.

For the following code section, the EX stage for MUL instructions requires 10 cycles. All other instructions' EX stages have only 1 cycle. Please note that SW instructions only write cache in CT stage.

```
1. MUL     R2, R11, R12
2. SW      R1, 0(R2)
3. LW      R3, 20(R4)
4. ADD     R5, R3, R6
5. LW      R7, 100(R8)
6. SUB     R9, R7, R8
7. ADDI    R10, R5, 20
```

1. If this pipeline employs the policy (A) mentioned above for memory dependence, show execution steps with timing for the above code section.

2. If this pipeline employs the policy (B) mentioned above for memory dependence, the memory dependence predictor predicts that there is no dependence for both loads. Two loads (inst. 3 and 5) are executed without stalls. However, after the store address generation, both instructions have true dependence with instruction 2, show execution steps with timing for the above code section.

3. Design a memory dependence predictor. The predictor would provide three predictions: dependence, no dependence, maybe. If the prediction were maybe the load would wait. Draw a diagram for your design and specify the circumstances for each prediction.

Consider a long, quiet country road with houses scattered very sparsely along it. (Picture this road as a long line segment, with an eastern endpoint and a western endpoint.) Further suppose that the residents of all these houses are demanding cell phone users. You want to place cell phone base stations at certain points along the road so that each house is within four kilometers of one of the base stations.

Describe an efficient algorithm that achieves this goal, using as few base stations as possible. Explain the correctness of your algorithm, and derive its time complexity in terms of the length of the road and the number of houses along it.

For each of the following two statements, decide whether it is true or false. If true, then explain why. If false, then give a counterexample.

(a) Let $G = (V, E)$ be an undirected, weighted graph with weight $w(u, v)$ on edge (u, v). Edge weights are all positive and distinct. Let T be a minimum spanning tree for G. Suppose we replace each edge weight $w(u, v) = c$ in G by its square c^2, creating a new instance G'. True or false: T must still be a minimum spanning tree for G'.

(b) Let $G = (V, E)$ be a directed, weighted graph with weight $w(u, v)$ on edge (u, v). Edge weights are all positive and distinct. Let P be a minimum-weight path from $s \in V$ to $t \in V$. Suppose we replace each edge weight $w(u, v) = c$ in G by its square c^2, creating a new instance G'. True or false: P must still be a minimum-weight path from s to t for G'.

Given two strings, the longest common substring (LCS) is a longest sequence of characters exists in both strings. For example, given string $S_1 = babcdefggg$ and string $S_2 = befabcdgfeeg$, their longest common substring is $abcd$.

a) Develop your most most efficient algorithm to compute the longest common substring between two given strings. Analyze your algorithm's space and time complexity.

b) Consider a slightly modified definition on LCS. Suppose now the common substring is allowed to have some different characters, as long as the different characters in the common string are not consecutive and are not at the beginning or ending position of the string. For example, the new LCS between S_1 and S_2 now becomes $abcdef$ of S_1, which matches with $abcdgf$ from S_2. Modify your algorithm to solve this problem. Make it efficient and analyze its space and time complexity.

Given two points $\mathbf{v}_1 = (x_1, y_1)$ and $\mathbf{v}_2 = (x_2, y_2)$, any point p located on line segment $[\mathbf{v}_1, \mathbf{v}_2]$ can be represented by:

$$p = (1 - \lambda)\mathbf{v}_1 + \lambda\mathbf{v}_2, \tag{1}$$

where $0 \leq \lambda \leq 1$ is called p's barycentric coordinate. The barycentric coordinate for any point between $\mathbf{v}_1$ and $\mathbf{v}_2$ is between 0 and 1, and it is linear with respect to $\mathbf{v}_1$ and $\mathbf{v}_2$.

(1) Now consider three non-collinear points $\mathbf{v}_1, \mathbf{v}_2, \mathbf{v}_3$, which forms a triangle $[\mathbf{v}_1, \mathbf{v}_2, \mathbf{v}_3]$. Any point p inside triangle $[\mathbf{v}_1, \mathbf{v}_2, \mathbf{v}_3]$ can also be represented using barycentric coordinates linearly that interpolates these three points. Derive the barycentric coordinates for a point inside the triangle. Note that coordinates should have each of its components ranging inside $[0, 1]$.

(2) Further generalize this barycentric coordinates to $n, (n > 3)$ points in n-dimensional space.

An image whose profile is given across an edge in Fig 1 is deteriorated with a white Gaussian noise.

i.   Propose an operator (single operator or composition of operators) that processes the image with a kernel-based function to reduce effect of the noise and to detect the edge.

ii.   What is the purpose of using this kernel-based function proposed; what type of a filter can it be?

iii.   How does your operator detect the edge pixel?

iv.   Illustrate your answers over the image profile.

v.   How can you increase computation performance of your operator for multiple images?
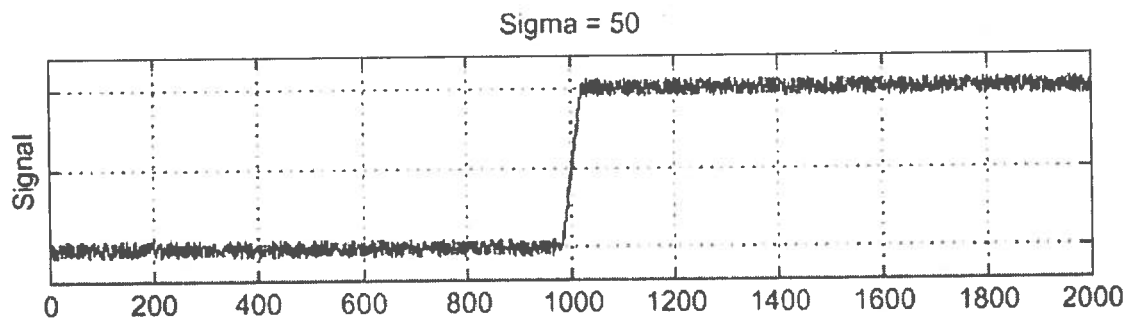
Fig 1 Image profile across an edge

Assume that an image is represented by its average image index *AvIndx* defined in equation (1). As an engineer you propose a similarity index, called normalized average image difference *NAID* defined in equation (2), between two images based on their *AvIndx*. You are asked to compare two images I_1 and I_2 whose elements are non-negative.

a. How would you test whether this method is 'robust' to a noise in the images compared?
b. What would be the relation between the *NAID* and a threshold *T* such that the proposed similarity measure is 'robust'? Explain your answer formally. State all assumptions you consider.

The proposed similarity measure: Two images are said to be dissimilar if their normalized average image difference *NAID* is greater than a threshold *T*. Hint: Signal = Original Signal + Noise.

$$AvIndx(I) = \frac{\sum_{x,y} I(x,y)}{N} \qquad\qquad (1)$$

$$NAID(I_1, I_2) = \frac{|AvIndx(I_1) - AvIndx(I_2)|}{\sum_{x,y} I_1(x,y) + I_2(x,y)} \qquad\qquad (2)$$

In the circuit below, all the diodes are identical, and conduct 1 mA with a forward voltage of 0.7 Volts. Initially there are 40 diodes in series.

1) If the voltage at B is 28 Volts, what is the voltage at A?

2) What is the impedance at B?

3) If there are only 39 diodes and the voltage at B is 28 Volts, what is the voltage at A?

4) What is the impedance at B?

5) If the voltage at B is 28 Volts and the voltage at A is 32 Volts, how many diodes are there?
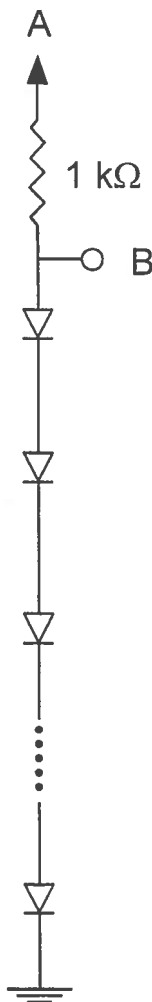
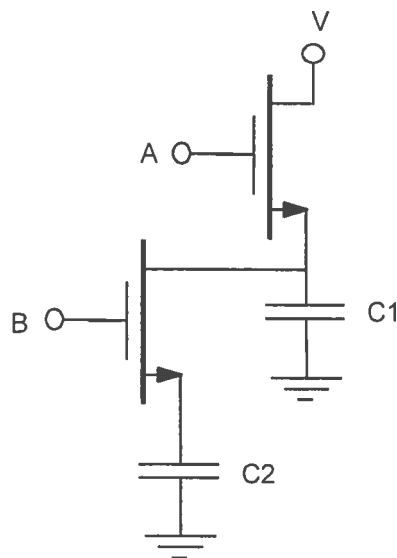## Circuits and Systems
Problem 2

In the circuit below the op-amps are ideal, and the diodes are identical with 0.7 Volt forward voltage.

a) If the input is at 0 Volts, find the voltages at A, B, and C.

b) If the input is at 1 Volt, find the voltages at A, B, and C.

c) Find the large signal gains for both positive and negative inputs.
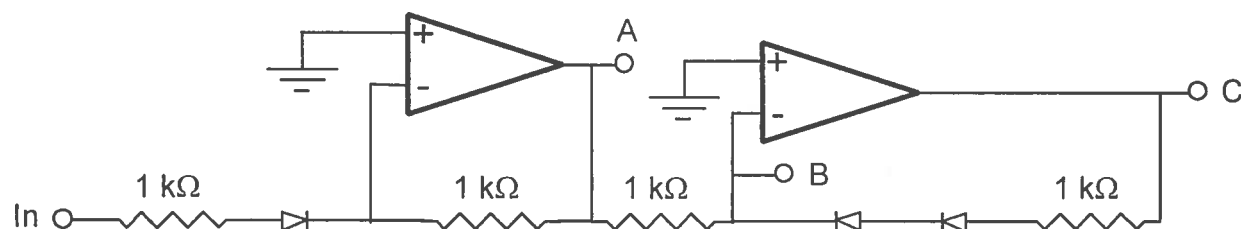
a) In the circuit below point A is initially positive and B is negative. The capacitor C1 is therefore charged to the voltage V. A is then held negative and B is made positive. What is the ratio between C1 and C2 so that C2 is charged to 0.001V?

b) The voltages on A and B are repetitively cycled, charging C1 to V and then discharging it into C2. How many charge-discharge cycles are required for the voltage on the larger capacitor to reach $(1-1/e)V$?

c) Choose a charge-discharge frequency so that the time for the voltage on the larger capacitor to reach $(1-1/e)V$ is 1 sec.

d) What is the equivalent resistance charging the larger capacitor?

Circuits and Systems
Problem 5

Consider the op-amp circuit shown below. Given, $V_{in} = V_0 \sin(\omega t)$ and open loop gain, $A_O = 10^5$. Assume ideal op-amps and answer the following questions.

(a) When the capacitor (C) is not connected, find an expression for the output voltage to the input voltage, V_{out}/V_{in}.

(b) Now consider the capacitor (C) is connected as shown in the circuit below. Find an expression for the current, I_C, in terms of V_{in} and V_{out}.

(c) Find an expression for I_C in terms of R_1 and R_2.

(d) Is it possible to determine effective impedance seen from the V_{in} terminal? If so, find the effective impedance. If not, explain why it is not possible to determine effective impedance.
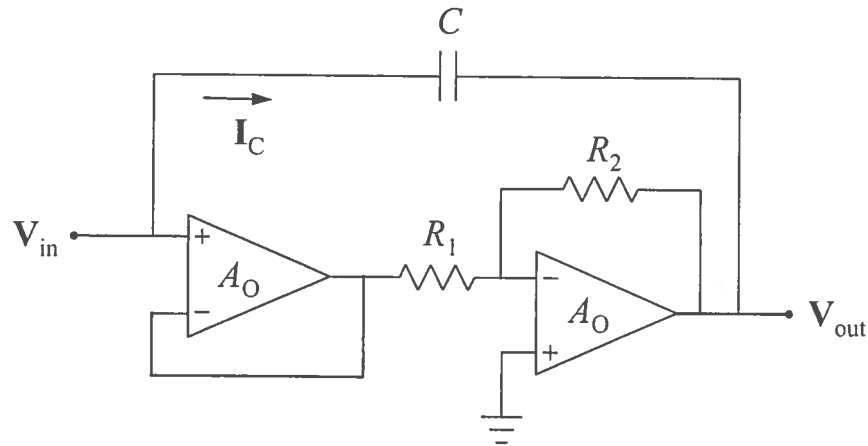
Physical Electronics

Problem 1

a) The following equation describes the relationship between the carrier concentration and the dopant concentration at room temperature, based on charge neutrality. Will the same equation be valid at extremely low temperature? Please justify your answer.

$$p - n + N_d - N_a = 0$$

b) Will the above equation be valid at high temperature (T=400K)? Please justify your answer.

c) A silicon is doped with Boron at a concentration of 10^{15} #/cm^3. What is the concentration of free electron and holes at 300K? Intrinsic carrier concentration $n_i = (9.15*10^{19})*(T/300)^2 * e^{-0.5928\,kT}$ and you can assume non-degeneracy. (you can assume $np=n_i^2$)

d) For the same silicon, what will be the concentration of free electron and holes at T=470K?

*. p, n, n_i, N_d, and N_a are hole concentration, free electron concentration, intrinsic carrier concentration, donor concentration, and acceptor concentration(#/cm^3) in a silicon. k is Boltzman constant and is $8.6*10^{-5}$ eV/K.

A silicon pn junction diode has the doping concentrations of $N_A = 2 \times 10^{16}$ cm^{-3} and $N_D = 5 \times 10^{15}$ cm^{-3}, respectively. Given, the intrinsic carrier concentration (n_i) is 1.45×10^{10} cm^{-3}, the Boltzmann constant (k) is 1.38×10^{-23} J/K, and the temperature (T) is 300 K. x_n and x_p are n-side and p-side widths of the depletion region.

(a) Draw an equilibrium band diagram.

(b) Assuming impurities are 100% ionized, <u>derive</u> the expression for the built-in potential at thermal equilibrium. Simply writing down the equation will not earn any credit.

(c) Calculate the built-in voltage (V_{bi}), the depletion region widths (x_n and x_p), and the maximum electric field (E_{max}).

(d) In (b), what would happen if the impurities are not 100% ionized? Would the resulting built-in potential be higher or lower, and why?

(e) When a reverse bias of 0.5 V is applied, repeat (c). In addition, calculate the junction capacitance. Assume the dielectric constant of silicon (ε_s) is 11.7.

Given a sample of silicon with n-type doping concentration, $N_D=10^{17}$ cm^{-3}.
Assume an electric field, E, of magnitude 1×10^3 V/cm is applied along the
sample in the +x direction. Use the figure below, as necessary. **Circle final
answers**.

a) Calculate the drift velocity for electrons. Indicate both magnitude and sign.

b) If an electron drifts a distance of 1 micron along this silicon sample, how long
will it take, on average, to drift this distance? (Show your calculation(s).)

c) Find the number of collisions that will occur over a distance of 1 micron.
(Assume a collision time of $\tau = 0.07$ picoseconds.)

d) Repeat part c) over a distance four (4) times the mean free path of electrons. Is
your answer valid? Explain—use no more than ½ page for your discussion.

mobility (cm²/Vs) vs $N_d + N_a$ total dopant concentration (cm^{-3})
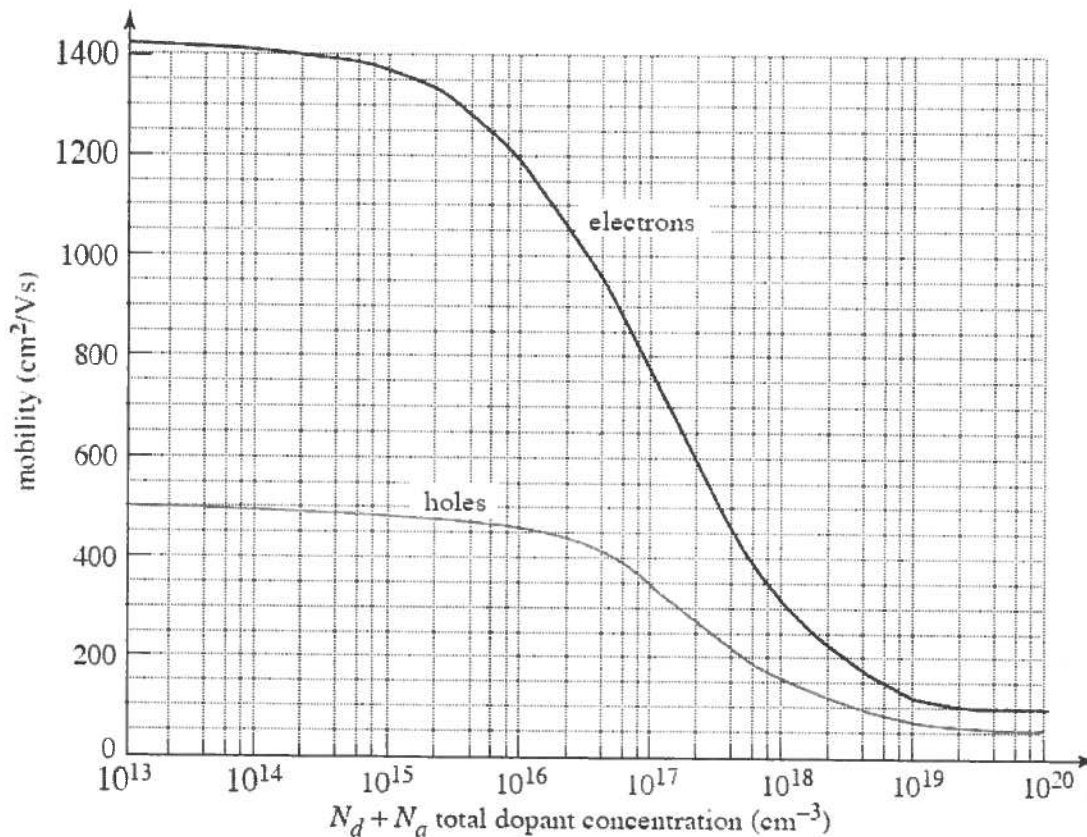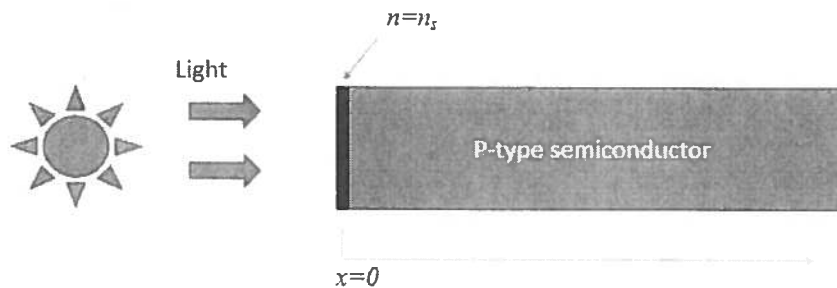
Physical Electronics

Problem 4

The following is a minority carrier diffusion equation for p-type semiconductor.

$$\frac{\partial \Delta n_p}{\partial t} = D_N \frac{\partial^2 \Delta n_p}{\partial x^2} - \frac{\Delta n_p}{\tau_n} + G_L$$

a) A piece of p-type silicon is uniformly illuminated with G_L. What is the steady-state concentration of the minority carrier?

b) A piece of silicon is uniformly illuminated with G_L until it reaches the stead-state condition. Then, the illumination is turned off at $t=0$. Derive the concentration of the minority carrier over time, $\Delta n_p(t)$.

c) Light is illuminated on one end of silicon bar as below, which is uniformly doped with $N_A=10^{15}$ #/cm^3. The light cannot penetrate into the silicon and affects only the surface(x=0). The concentration of the free electron at the illuminated side is measured to be n_s. Derive $n(x)$, the free electron concentration, along the length of the silicon bar in a steady-state condition.

$n=n_s$

Light

P-type semiconductor

$x=0$

*. Δn_p is an excessive minority carrier concentration, defined as $n - n_0$, where n, n_0 are the free electron concentration, and the equilibrium electron concentration. D_n is the minority carrier diffusivity; τ is minority carrier lifetime.

The magnetic field phasor of a uniform plane wave propagating in free space is given by

$$\mathbf{H}(z) = H_0 e^{-jk_0 z} \hat{\mathbf{y}}.$$

(a) Calculate the left side of Ampere's law $\oint \mathbf{H} \cdot d\mathbf{L} = \int_S \mathbf{J}_d \cdot d\mathbf{S}$ for the surface $x = 0$, $0 \le y \le \dfrac{\lambda}{2}$, $0 \le z \le \dfrac{\lambda}{2}$ (shown in the figure below), where $\lambda = \dfrac{2\pi}{k_0}$ is the wavelength, and $\mathbf{J}_d = j\omega \mathbf{D}$ is the displacement current density.

(b) Calculate the electric flux density $\mathbf{D}$, and use it to calculate the right side of Ampere's law.
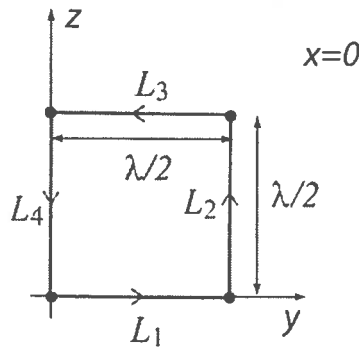
Consider a unity negative feedback system with a plant model given by

$$P(s) = \frac{10(s-5)}{s(s^2 + s + 4)}$$

and a controller given by

$$C(s) = \frac{K(s+b)}{s+a}$$

for some $K > 0$ and some real b and a.

1. Use root locus method to determine the signs of b and a so that the closed-loop system is stable for all $K \in (0, K_u)$ for some $K_u > 0$.

2. Sketch the possible forms of root locus in terms of the pole and zero location of $C(s)$.

Consider the continuous-time signal waveform

$$s(t) = \sum_{k=0}^{n-1} c_k\, p(t - kT_c),$$

where $T_c > 0$ and $p(t) = \begin{cases} 1, & \text{if } 0 \le t < T_c \\ 0, & \text{otherwise} \end{cases}$.

1. If $\{c_0, c_1, \ldots, c_{n-1}\}$ is a given (deterministic) sequence, determine the signal spectrum $S(j\Omega) = \mathcal{F}\{s(t)\} = \int_{-\infty}^{\infty} s(t)\, \exp(-j\Omega t)\, dt$ in terms of c_k, T_c, and Ω, where $j = \sqrt{-1}$.

2. If the symbol period is $T_b = nT_c$, what is the frequency response for the matched filter, i.e., $S_{\text{match}}(j\Omega) = \mathcal{F}\{s(T_b - t)\}$ in terms of c_k, T_c, and Ω?

3. According to Part 2, determine the value of the output of the matched filter at the instant $t = nT_c$ in terms of c_k, T_c, and n.

The unit-step input signal $u(n)$ is defined as 1 for $n \geq 0$ and 0 for $n < 0$. Consider a causal, linear and time-invariant (LTI) system whose input signal is given by $x(n) = u(n)$ and whose output signal is given by

$$y(n) = 2^n u(-n - 1) - (0.5)^n u(n).$$

1. Determine the impulse response $h(n)$ of this LTI system.

2. Find the transfer function $H(z)$.

3. Determine whether the LTI system is stable or not, in a bounded-input bounded-output (BIBO) sense.

4. If the LTI system has the input signal $x(n) = 2^n u(n) + u(-n)$, determine the corresponding output signal $y(n)$.

Let $\{X_t; -\infty < t < \infty\}$ be a Gaussian random process with $E\{X_t\} = 0$ for all t and

$$E\{X_t\, X_s\} = \frac{1}{2}\left(|t| + |s| - |t - s|\right).$$

1. Write the probability density function (PDF) of the random variable X_t for $t = 1$, and $t = -1$.

2. Write the joint PDF of X_t and X_{-s} for $t > 0$ and $s > 0$.

3. What conclusion can you draw for the segments $\{X_t; t \geq 0\}$ and $\{X_t; t < 0\}$ of the process.

4. The process $\{X(t)\}$ is used to modulate a carrier signal at frequency f_0 to get

$$Y(t) = X(t)\cos(2\pi f_0 t + \Theta)$$

where f_0 is constant and Θ is independent of $\{X(t)\}$ and is uniformly distributed over the interval $[0, 2\pi)$. Find the mean and autocorrelation functions of the process $\{Y(t)\}$.

Signals $x(t)$ and $y(t)$ are both periodic with period T. Let $\{x_n\}$ and $\{y_n\}$ denote the Fourier series for $x(t)$ and $y(t)$, respectively.

1. Write the Fourier series pair of equations relating $x(t)$ and $\{x_n\}$.

2. Prove the equality
$$\int_{-T/2}^{T/2} x(t)y^*(t)dt = \sum_{n=-\infty}^{\infty} x_n y_n^* \tag{0.1}$$

3. Using (0.1) prove the Parseval's theorem and interpret it.

4. $g(t)$ is a function of duration T_0 over the interval $[-T_0/2, T_0/2]$. Let $f_0 = 1/T_0$. Prove the following identity referred to as *Poisson's sum formula*.

$$\sum_{m=-\infty}^{\infty} g(t - mT_0) = f_0 \sum_{n=-\infty}^{\infty} G(nf_0)e^{j2\pi n f_0 t} \tag{0.2}$$

where $G(f)$ is the Fourier transform of $g(t)$.

Consider a sequence of K identically and independently distributed Bernoulli random variables $\{X_n, n = 0, 1, \cdots, K-1\}$ with $P(X_n = 1) = 1 - P(X_n = 0) = \alpha \in (0, 1)$ for all n. Let $S_K = \sum_{n=0}^{K-1} X_n$ denote the weight of the sequence, namely, total number of 1's observed in the sequence. Answer the following questions:

1. Compute $P\{X_0 = x_0, X_1 = x_1, \cdots, X_{K-1} = x_{K-1}\}$, the probability of any sequence of K binary variables, with $x_j \in \{0, 1\}$ for all j, and express it as a function of its total weight S_K.

2. Find the probability mass function (PMF) of S_K, i.e. $P(S_K = j)$ for all possible j's.

3. Given $S_K = L \leq K$, find the conditional probability mass function of the sequence $\{X_n\}$, i.e. $P\{X_0 = x_0, X_1 = x_1, \cdots, X_{K-1} = x_{K-1} | S_K = L\}$. Does this conditional probability depend on the parameter α?

4. Assume $\alpha = 0.3$, and we divide all possible binary sequences of K binary symbols into different classes in terms of S_K, i.e. all sequences whose total weight is $S_K = L \leq K$ are put into the L-th class. Among all these classes, which class has the largest probability for large K? (Justify your answer)