MS Comprehensive / Ph.D. Qualifying Exam

# Automatic Control Topics

**A.  Basic Tools**
Laplace, Z transforms: basic properties, use in solving linear differential/difference equations, application to system analysis, transfer functions.  Fourier transform, Fourier series:  basic properties, application to signal analysis, frequency response, spectral energy density.

**B.  Basic Concepts**
Linearity, time invariance, causality, difference and differential systems, linearization, signal-flow and block diagrams, BIBO and asymptotic stability.

**C.  Classical Control**
Transient and steady state analysis and performance indicators, pole location, sensitivity; frequency domain analysis, phase and gain margins; Nyquist stability, Routh-Hourwitz criterion, root locus, lead and lag compensator design, PID control; pole placement with fractional controllers.

**D.  Sampled Data Systems**
Basic A/D and D/A conversion, sampling theorem.  Discretization of continuous time systems, deadbeat control.

**E.  State Space Control for  Continuous and Discrete Time Systems**
State and state equations, transition matrix, solution of state equation. Realization, controllability and stabilizability, observability and detectability, Lyapunov stability, state feedback and pole placement, asymptotic observers, state feedback with observers.

## Representative References

1.  C-T. Chen, *System and Signal Analysis*, Saunders College Publishing.
2.  B.C. Kuo, *Automatic Control Systems*, Prentice Hall.
3.  G.F. Franklin, J.D. Powell, A. Emami-Naeini, *Feedback Control of Linear Systems*, Addison Wesley.
4.  G.F. Franklin, J.D. Powell, M.L. Workman, *Digital Control of Dynamic Systems*, Addison Wesley.
5.  K. Ogata, *Discrete-time Control Systems*, Prentice Hall.
6.  W.L. Brogan, *Modern Control Theory*, Quantum Publishers, Inc.
7.  T. Kailath, *Linear Systems*, Prentice Hall.
8.  K. Ogata, *Modern Control Engineering*, Prentice Hall.
9.  C. T. Chen, *Linear system Theory and Design*, 3rd Ed., Oxford University Press, 1999.

# M.S. Comprehensive /Ph.D. Qualifying Exam
## Communication and Signal Processing Topics

**Probability Theory and Random Processes**

Basic concepts in probability theory; stationarity and wide sense stationarity of random processes, power spectral density, linear filtering of random processes, minimum mean squared error estimation, Gaussian and Poisson random processes.

**Signals, Systems, and Digital Signal Processing**

Continuous time and discrete time signals and systems: fundamental concepts, system properties (causality, stability, time invariance, etc.); time and frequency domain characterization of discrete and continuous time signals and systems; transform domain techniques; sampling and reconstruction; sampling rate conversion, frequency-domain analysis, aliasing and Nyquist rate concepts; discrete Fourier Transform and FFT algorithms; design and implementation of FIR and IIR filters.

**Analog  Communication**

Amplitude modulation techniques; frequency and phase modulation techniques; sampling, quantization; pulse code modulation (PCM); effect of noise on continuous wave and PCM systems.

**Digital Communication**

 Signal space representation; baseband representation of bandpass signals and systems; maximum likelihood (ML) detection and estimation; optimum receiver principles. performance of optimum receivers; differential, partially coherent and non-coherent detection of signals; bandwidth efficiency and power efficiency; receiver design and performance analysis of digital modulation schemes in fading channels; linear block codes and their decoding strategies, hard decision and soft decision decoding.

## Representative References

1.  Simon Haykin, *Communications Systems*, (Wiley).
2.  J. G. Proakis and M. Salehi, *Communication Systems Engineering, 2nd Edition*, Prentice Hall.
3.  J. G. Proakis, *Digital Communication*, 4th Edition, McGraw-Hill, 2000.
4.  J. M. Wopzencraft and I. M. Jacobs,  *Principles of Communication Engineering*, John Wiley & Sons, New York, 1965.
5.  Henry Stark and John W. Woods, *Probability and Random Processes with Applications to Signal Processing, 3rd Edition.* Prentice-Hall.
6.  *Probability, Random Variables, and Stochastic Processes*, A. Papoulis, 3rd edition, McGraw-Hill, 1991.
7.  S. K. Mitra, *Digital Signal Processing*, 3rd edition, McGraw-Hill.
8.  A. V. Oppenheim and R.W. Schafer, *Discrete-time Signal Processing*, Prentice-Hall.

**MS COMPREHENSIVE / PHD QUALIFYING EXAM**

# COMPUTER ENGINEERING TOPICS

Appearing below is an outline of topics which computer-area questions will be based on. Most of the topics clearly fall into one of the three question areas, Hardware, Software, and Applications, but questions in one area can draw on topics from other areas. For example, the solution to an algorithm (software) question might require knowledge of cache organization (hardware).

Topics described with "Proficiency in" (or similar wording) must be understood very well, as though you were going to take a test in a course covering the topic. Topics described using "Competence with" (or similar wording) must be understood well enough to solve problems or answer substantive questions, however definitions or other background might be provided as part of the question. This information should help students that know the material make a quick start solving the problem. For topics listed under "Familiarity with" students should have a basic background in the area, including basic terminology, but need not know many specifics. For these problems a greater amount of background will be provided, enough so that a good student might be able to solve them without having taken any courses covering the topic.

## Logic Design
Proficiency with combinational and sequential logic theory at EE 2720 and EE 2730 level, including Boolean algebra and basic minimization techniques. Proficiency in designing basic combinational and sequential circuits.

## Computer Arithmetic
Proficiency with signed integer representations and with full adder and carry look-ahead adder designs. Competence with basic integer multiplication and division circuits. Competence with floating-point (FP) representations, including IEEE 754, and with FP arithmetic. Familiarity with modular and residue arithmetic.

## Computer Instruction-Set Architecture (ISA) and Microarchitecture
Proficiency with 5-staged pipelined RISC (e.g., MIPS) implementations, including design rationale, direct and bypassed data paths, control signals, and relationship between implementation and instructions. Competence in assembly language programming, including RISC instruction sets. Competence with instruction set design issues, including memory addressing modes, and the variety of jumps & branch instructions. Familiarity with interrupts, traps, and exceptions. Familiarity with pipeline depth and superscalar width issues. Familiarity with caches and branch prediction techniques.

## Computer Communication Networks
Competence with basic switching and multiplexing techniques. Familiarity with network layers and protocol stacks, ARQ protocols, error detection and correction. Familiarity with Internet addressing and routing standards and techniques. Familiarity with network reliability, availability, structural reliability terminology and techniques.

## Algorithms and Data Structures
Proficiency with basic data structures (including arrays, stacks, linked lists, trees), basic algorithms (including binary search, merge sort, tree searches), memory content and layout of numbers, pointers, arrays, and structures complexity analysis of algorithms. Competence with advanced data structures (including hash tables, graph representations), algorithmic paradigms (including divide and-conquer, greedy, dynamic programming) and analysis techniques (including recurrence relations, amortized analysis). Familiarity with computational complexity and intractability randomized, online and approximation algorithms.

## Parallel and Distributed Computing
Competence in major parallel system organization topics including hardware organizations (CPU & network), parallel program organizations (processes, tasks, or threads), communication models (message passing or shared memory). Competence with metrics for analysis of performance including speedup, efficiency, time complexity, and space complexity. Competence with use and implementation of basic synchronization primitives and constructs including compare & swap, atomic memory operations, semaphores, and barriers. Competence with basic parallel algorithms including reduction, sorting, leader election, graph algs, etc. Competence with common interconnects including bus, crossbar, mesh, hypercube networks.
Familiarity with other interconnects including Log n stage networks (e.g., omega), Clos and Benes networks.

## Operating Systems and Compilers
Competence with coordination concepts, constructs, and issues, including multiple-process access to shared structures, mutual exclusion, and deadlock. (See also basic synchronization topics under Parallel and distributed computing.) Competence with basic memory management issues including virtual and physical addresses and their rationale virtual to physical address translation techniques, page swapping basics. Competence with program compilation techniques, including control-flow and data-flow program representations, dependencies and dependence testing, common optimizations, and common program transformations.

## Computer Vision and Image Processing
Proficiency in geometric and radiometric image formation. Proficiency in image segmentation, enhancement and restoration techniques. Competence in image compression and morphological image processing. Familiarity with pattern recognition techniques.

## Logic Testing and Reliability
Familiarity with fault models, including the stuck-at model.

March 4, 2010

MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

# ELECTRONICS ENGINEERING TOPICS

**A. Circuits**

Circuit applications of diodes. Circuit applications of BJT, MOSFETs and JFETs in linear and digital circuits. Linear applications include amplifiers, oscillators, differential amplifiers and operational amplifiers. Applications of ideal operational amplifiers. Digital applications include internal operation of standard logic gates used as building blocks in logic families such as TTL, ECL, NMOS and CMOS.

**B. Devices**

Basics of carrier transport in semiconductor materials, physics of p-n junction diodes, bipolar and field effect transistors. Derivation of terminal current-voltage characteristics of discrete devices, large and small signal models. Basic physics of photonic devices. Basic integrated circuit technology.

**C. Fields**

Static fields, Maxwell's equations, propagation through istropic medium, reflections and basic antenna theory.

## Representative References

1. M.N. Horenstein, *Microelectronic Circuit and Devices*, Prentice Hall.
2. Mitchell & Mitchell, *Introduction to Electronic Design*, 2nd Ed., Prentice Hall.
3. Gray & Mayer, *Analysis and Design of Analog Integrated Circuits*, 3rd Ed., John Wiley.
4. D. A. Hodges, H. G. Jackson and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, 3rd Ed., McGraw-Hill.
5. B. Streetman, *Solid State Electronic Devices*, 3rd Ed., Prentice Hall.
6. J.P. McKelvey, *Solid State and Semiconductor Physics*, Harper & Row.
7. Shen, *Applied Electromagnetics*, 2nd Ed., Prindle-Weber-Schmidt.

# COMPREHENSIVE MS/QUALIFYING PH.D. EXAM

## POWER ENGINEERING TOPICS

A.  Electric Machinery
    Maxwell's equations; analysis of simple electromechanical devices using Maxwell's equations; synchronous machines, voltage behind reactance model, Park transformation, d,q equations; exact and approximate equivalent circuits of single-phase transformers, nonlinear effects; modeling and calculation of its parameters of transmission lines; modeling and analysis of direct current and induction machines.

B.  Power Systems
    Per-unit calculations; symmetrical components; sequence impedances of transformers, synchronous machines and induction motors, sequence impedances and capacitances of transmission lines; sequence networks for fault analysis; shunt faults (3-phase, LG, LLG, LL faults); series faults (1LO, 2LO); power flow equations, (Decoupled) Newton-Raphson, Gauss/Gauss-Seidel methods; optimal dispatch with/without line losses; transient stability, swing equation, equal area criterion, effect of clearing time; low-frequency oscillations, supplementary excitation/governor control; linear optimal stabilization.

C.  Power Electronics
    Fourier series of nonsinusoidal voltages and currents; analysis of circuits with nonsinusoidal voltage and current waveforms, nonsinusoidal active and apparent powers; single-phase and three-phase rectifiers, controlled AC/DC converters, DC/DC converters, inverters.

## Representative References

1. R.D. Schultz & R.A. Smith, *Introduction to Electric Power Engineering,* John Wiley, 1988.
2. V. DelToro, *Electric Power Systems*, Prentice Hall, 1992.
3. P.M. Andersen, *Analysis of Faulted Power Systems*, The Iowa State Univ. Press, 1983.
4. Y.N. Yu, *Electric Power System Dynamics*, Academic Press, 1983.
5. M.H. Rashid, *Power Electronics*, Prentice Hall, 1988.
6. N. Mohan, T.M. Undeland, W.P. Robbins, *Power Electronics*, John Wiley, 1989.

This question is regarding to cache design.

(a) For the same cache size, is it possible for a direct-mapped cache having a better hit rate than a fully associative cache? If so, give an example for the access pattern or the program using the caches; if not, justify the reason.

(b) For the same cache with different replacement policies, is it possible for the cache with the least-recently-used (LRU) policy having a better hit rate than the optimal (OPT) replacement policy? If so, give an example for the access pattern; otherwise, explain why not?

(c) For a dual-core processor, there is a shared last level cache between the two cores. Two threads (T1 and T2) can run either individually or simultaneously. When the threads running individually, the last level cache hit ratio for the two threads (T1 and T2) are H1 and H2 respectively. When the threads running simultaneously, the last level cache hit ratio for the two threads (T1 and T2) is H1' and H2' respectively. Is it possible for H1' > H1 and H2' > H2? If yes, list an example for the access patterns or write the programs; otherwise, justify your answer.

Usually, we have two policies for memory disambiguation in an out-of-order executed processor: (1) a conservative solution is stalling a load instruction and its dependent instructions until the early store's address generation; (2) another alternative is predicting the memory dependence between loads and earlier outstanding stores. Memory dependence prediction allows loads to bypass earlier stores if no dependence is predicted. Otherwise, if dependence is predicted, load values can be forwarded from the latest earlier stores without cache access. At the commit stage of stores, the processor check correctness of predictions, if not, loads and their dependent instructions would be re-executed.

Now consider a two-issue, out-of-order execution pipeline with following stages: Instruction Fetch (IF), Decode (ID), Issue (IS), Execution / Address Generation (EX), Write Result (WR), Commit (CT). There are two integer ALU units, two load/store units and one MUL unit.

For the following code section, the EX stage for MUL instructions requires 10 cycles. All other instructions' EX stages have only 1 cycle. Please note that SW instructions only write cache in CT stage.

| | | |
|---|---|---|
| 1. MUL | R2, R11, R12 |
| 2. SW | R1, 0(R2) |
| 3. LW | R3, 20(R4) |
| 4. ADD | R5, R3, R6 |
| 5. LW | R7, 100(R8) |
| 6. SUB | R9, R7, R8 |
| 7. ADDI | R10, R5, 20 |

(a) If this pipeline employs the policy (1) mentioned above for memory dependence, show execution steps with timing for the above code section.

(b) If this pipeline employs the policy (2) mentioned above for memory dependence, the memory dependence predictor predicts that there is no dependence for both loads. Two loads (inst. 3 and 5) are executed without stalls. However, after the store address generation, instruction 3 has a true dependence with instruction 2 but instruction 5 doesn't have, show execution steps with timing for the above code section.

(c) Design a memory dependence predictor. The predictor would provide two predictions: dependence, no dependence. Draw a diagram for your design and specify the circumstances for each prediction.

Let $*$ be any associative binary operation. The *prefix computation* (with respect to $*$) on an array $A = \langle a_0, a_1, \cdots, a_{n-1} \rangle$ produces a second array $B = \langle b_0, b_1, \cdots, b_{n-1} \rangle$, where $b_i = a_0 * a_1 * \cdots * a_i$, for any $0 \le i < n$. The figure below shows prefix computation circuits for $n = 4$ and 8. In these figures, each box represents hardware for applying $*$ to its two inputs.
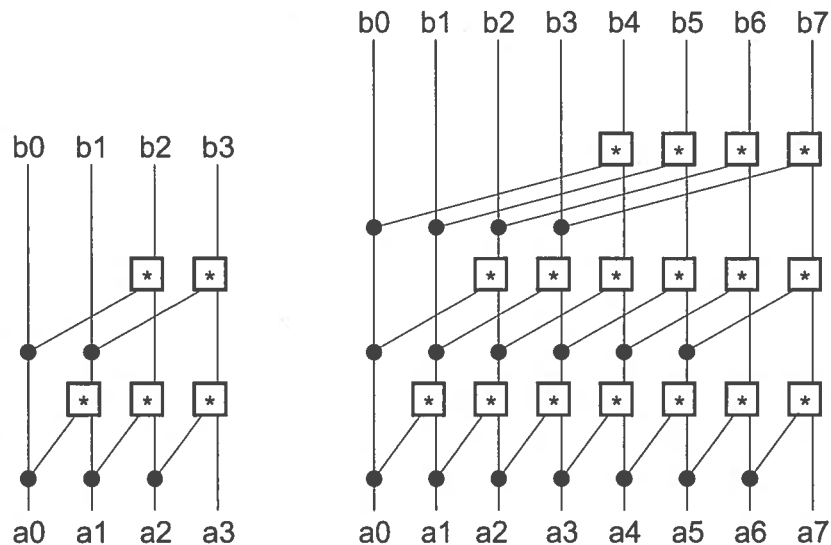


(a) Draw a similar prefix computing circuit for 16 inputs.

(b) Adapt the given circuit for 8 inputs to work for 5 inputs.

(c) Describe the circuit for the general case of $n = 2^k$ inputs, and prove that it correctly performs the prefix computation.

(d) Observe that adding 1 to an $n$-bit number amounts to complementing all lower order bits up to the first 0. For example, $10110 \; 0111111 + 1 = \overbrace{10110}^{\text{unchanged}} \; \underbrace{1000000}_{\text{complemented}}$ .

An $n$-bit binary counter counts up from 0 to $2^n - 1$ and then back to 0. Describe how a fast prefix computing circuit can help build a fast counter.

(a) "In the field of computer science, a binary decision diagram (**BDD**) or a propositional directed acyclic graph (PDAG) is a data structure that is used to represent a Boolean function The data structure is created using the *Shannon expansion* where a switching function is split into two sub-functions (cofactors) by assigning one variable (cf. *if-then-else normal form*). [Wikipedia]."
For example, the BDD for an AND gate with inputs x1 and x2 is as follows:
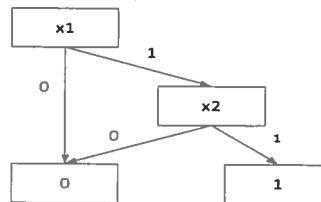


BDD for a 2-input AND gate

Using this concept, show the BDD for a (i) 2-input OR gate with inputs x1 and x2 and (ii) 1-bit Full Adder with inputs $A_i$, $B_i$, and $C_{in}$ and outputs $S_i$ and $C_{out}$.

(b) In the figure shown above (BDD for a 2-input AND gate), if each event ($x_i$ as 1 or 0) is equally likely, find the probability of (a) output being 1 and (b) output being 0. What will happen to (b) if the probability of $x_i$ being 1 changes to ¾ ?

Assume that there is a processor using Tomasulo's algorithm with a reorder buffer to enforce in-order commit for handling misprediction and exception. It has the following execution stages: instruction fetch (IF), issue (IS), execute (EX), memory (ME), write result (WI) and commit (CM). Each stage takes *one* cycle except for MULTD's EX stage (5 cycles) and the ME stages. Load/Store takes 1 cycle to compute address (EX) and 2 cycles for memory access (ME). Note that only Load/Store has the ME stage. Load that depends on a store can only access cache after the store commits and put the data into cache. The dependent instruction cannot start execution until the cycle after the WI stage of the source instruction. The processor is a two-issue superscalar processor with only one common-data-bus (CDB). Two instructions (on top of the reorder buffer) can be committed at the same cycle. There are only 6 entries in the reorder buffer. It has the following functional units: one integer unit, one ADDD/SUBD unit, one MULTD unit, one address calculation unit and one memory unit for LD/SD.

(a) Simulate the execution of the following code segment using the table provided. Use '-' to indicate a stall cycle wherever applied. Use more tables if necessary.

```
(1)    LD      F6,0(R1)          //Load Double
(2)    LD      F2,0(R2)
(3)    MULTD   F0,F2,F4          //Multiplication Double
(4)    ADDD    F10,F2,F6         //Add Double
(5)    SD      F10,0(R3)         //Store Double
(6)    SUBD    F12,F6,F2
(7)    LD      F8,0(R3)
(8)    SD      F8,0(R2)
```

| time | t1 | t2 | t3 | t4 | t5 | t6 | t7 | t8 | t9 | t10 | ... | ... | | | |
|------|----|----|----|----|----|----|----|----|----|-----|-----|-----|--|--|--|
| (1)  | IF | IS | EX | ME | ME | WI | CM | | | | | | | | |
| (2)  | IF | IS | | | | | | | | | | | | | |
| (3)  | | IF | | | | | | | | | | | | | |
| (4)  | | | | | | | | | | | | | | | |
| (5)  | | | | | | | | | | | | | | | |
| (6)  | | | | | | | | | | | | | | | |
| (7)  | | | | | | | | | | | | | | | |
| (8)  | | | | | | | | | | | | | | | |

(b). Assume the above processor is enhanced with a load value prediction hardware. With this scheme, load instructions can speculatively obtain their values after the instruction fetch (IF) stage. Therefore the load dependent instructions can execute with the speculative value smoothly and the pipeline doesn't stall. At the beginning of the load's WI stage, the processor will check between the true data value fetched from memory and the speculative value. For the above code in part (b), if instruction 1 and 7 get the *wrong* value from the prediction hardware and the instruction 2 gets the *correct* value, complete the pipeline diagram showing the execution of the code. Devise a reasonable recovery method and show the execution procedure in the diagram. You need pay attention to avoid the structural hazard. You also must use the format in part (a).

Consider a mesh topology, in which each node (or processor) is connected to its neighbors to the North, South, East and West (if they exist) by full-duplex bidirectional links. Each processor is sending message(s) to other processors. The message destinations could be arbitrary and the number and length of messages, while is finite, is unrestricted. For the model used in this problem, a message from processor $p_{i,j}$ (in row $i$, column $j$) to processor $p_{\ell,m}$ follows some path dictated by a "routing strategy." Once this path has been established, the message (which could be quite long) follows this path from the source to the destination. There are two restrictions to the message flow:

- Each link can carry only one message at a time.

- Once a link starts on a message, it must convey the entire message before it can move to another message.

This problem deals with deadlocks that can arise if the routing strategy is not properly managed. That is, a "cycle of messages" could be waiting on each other for a link.

(a)    If there is no restriction on the routing strategy, give an example to show that a deadlock is possible.

(b)    Suppose each message from $p_{i,j}$ to $p_{\ell,m}$ is restricted to follow the routing strategy below (dimension ordered routing):

   The message first moves on row $i$ in the correct direction until it comes to column $m$, then it moves along column $m$ in the right direction until it reaches row $\ell$.

   Show that this routing strategy can never cause a deadlock.

(c)    What is a major disadvantage of the above strategy? Construct an example to illustrate this disadvantage.

Consider the MIPS code below which contains multiple branches that jump very far away, too far for MIPS instructions' 16-bit displacement. (Because of the oversize displacement there would be an assembler error for this code.) All of these branch instructions jump to targets within 4096 bytes of each other (but far away from the address of the branch instruction itself).

```
CODE_REGION_1: # Address = 0x1000
        bgtz r1,  FAR_AWAY_1   # Branch if register r1 > 0.
        add r2, r2, r3
        bltz r2,  FAR_AWAY_2   # Branch if register r2 < 0.
        and r2, r2, r4
        beqz r2,  FAR_AWAY_3   # Branch if register r2 = 0.
        sub r5, r6, r7
# More of Code Region 1 Here.


# Far-Away Code Region Below
FAR_AWAY_1:# Addr=0x12340010
        xor r10, r11, r12
        # More code here.

FAR_AWAY_2:# Addr=0x12340200
        or r10, r11, r12
        # More code here.

FAR_AWAY_3:# Addr=0x12340314
        lw r20, 0(r21)
        # More code here.
```
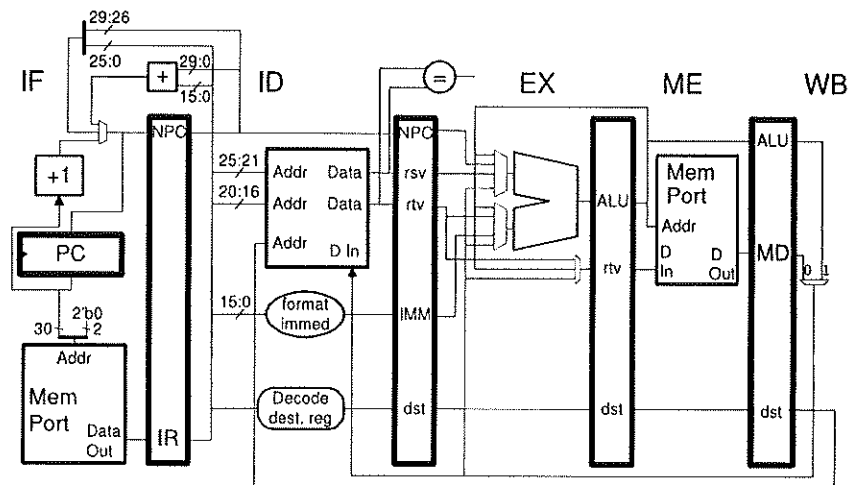


Design new branch instructions to accommodate these branches. The target address should be computed using some combination of a general-purpose (integer) register value and some kind of displacement. The new branch instructions will use a single register as a condition, branching if the value is zero, negative, or positive, depending on the instruction.

(a) Modify the hardware above for these new branch instructions. In your solution be clear about what your hardware connects to, using stage names like IF and ID if necessary.

- A priority is to not increase the length of the critical path.

- Take advantage of the fact that the smallest address in our example was 0x12340010 and not 0x1233fffc.

- Show both the hardware that computes the branch condition.

- Show the hardware that computes the branch target address.

(b) Show the coding for the new branch instructions.

The routine below accesses huge_array, which has a very large number of elements. Though large, only a small subset of elements is accessed. That is, the set of possible values of i that will be encountered in a run of the program will be much smaller than the size of huge_array, though still large enough so that there are many cache misses.

```
int something(int i) {
  int x = huge_array[i];
  return x;
}
```

The set of values has the following property: when looked at in sorted order some values are close together, for example, 1000, 1002, 1003, while others are far apart, for example, 1234000, 9999000, 72888123. We would expect element 1002 to share a cache line with 1000 or 1003 or both, but each of the far apart elements would be alone on a cache line.

Consider the design of a set-associative cache for code like this. The replacement decision would be based on the number of elements in the cache line that had been accessed, rather than the common least-recently used (LRU) policy. That is, if there are two lines in a set, one with 5 accessed elements and one with 1 accessed element, the line with 1 accessed element would be replaced, even if the 5-element line was less-recently used.

(a) Describe the additional data that is needed in the tag store for this scheme. Assume that the cache can see the size of the data item being fetched by the CPU.

- Describe what the data is.

- Indicate the size of the data needed in the tag store, as a percentage of the cache capacity.

- Indicate any assumptions.

(b) One problem with this scheme is what to do on a miss when all of the lines in a set have more than one accessed element. The line being brought in has just one accessed element (by the access causing the miss), so should it replace a line in the set with, say two accessed elements, in the hope that the new line will later have more elements accessed. Describe a possible solution to this problem.

(c) Assume the a good solution to the replacement problem in the last part was found (not necessarily your own answer). Would this scheme work better than LRU if the values of i have some temporal locality? Explain your answer. (The sequence of accesses values of i *temporal locality* if the probability of a particular value of i (say 1000) appearing is higher if it appeared recently and lower if it has not appeared for a long time.)

(a) An undirected graph $G = (V, E)$ is said to be *connected* if for all pairs of vertices $a \in V$ and $b \in V$, there is a path between $a$ and $b$. Design an efficient sequential algorithm to determine if an undirected graph is connected. **You will lose points if your algorithm is not efficient.** Prove its correctness. Analyze its running time. Is your algorithm the most efficient sequential algorithm one can design for this problem? Explain.

(b) A directed graph $G = (V, E)$ is said to be *strongly connected* if for all pairs of vertices $a \in V$ and $b \in V$, there is a path from $a$ and $b$ and there is a path from $b$ to $a$. Design an efficient sequential algorithm to determine if a directed graph is strongly connected. **You will lose points if your algorithm is not efficient.** Prove its correctness. Analyze its running time. Is your algorithm the most efficient sequential algorithm one can design for this problem? Explain.

# Computer Software 2

Describe a range $r$ as $[p_0, p_1]$, where $p_0$ and $p_1$ are integers such that $0 \le p_0 < p_1 < u$. Define a *normalized range* to be a range $q = [n_0, n_1]$ such that $n_0$ is a multiple of a power of 2, say $2^b$ (so $n_0 = i \cdot 2^b$ for an integer $i$), and $n_1 = n_0 + 2^b - 1$. For example, $[12, 15]$ is a normalized range for $2^2$.

(a) What is the largest normalized range contained in the range $[50, 100]$? Note that you may consider any power of 2.

(b) Consider an arbitrary range $r = [p_0, p_1]$ and the largest normalized range $q = [n_0, n_1]$ contained in $r$. (That is, $p_0 \le n_0 < n_1 \le p_1$.) What is the lower bound on the ratio $|r| / |q|$? What is the upper bound on the ratio $|r| / |q|$? Explain your reasoning.

Consider a distributed system represented by a graph $\mathcal{G} = (V, E)$. The graph has $n$ nodes, $m$ edges, degree $\delta$ and diameter $D$. Each node is aware only of its own neighbors; it may not be even be aware of the underlying topology $\mathcal{G}$ or values of $n$, $m$, $\delta$ or $D$.

Algorithms on this distributed system have the following structure. Initially, all nodes are asleep. A set of *starting nodes* spontaneously wakes up and starts the algorithm. Other nodes wake up and participate in the algorithm on receiving a message from a neighbor. A node can receive one or more messages from its neighbors, perform some internal operation and send messages to one or more of its neighbors. For this problem we do not restrict the length of messages or the local computation. When a node has finished its part in the algorithm, it goes back to sleep. A node that has gone back to sleep cannot wake up again during the algorithm. The entire algorithm terminates when all nodes have gone back to sleep. Further, the last node that goes to sleep must be a starting node.

The system operates asynchronously with all actions of a node being event driven (either on waking up or on receiving a message). While message latencies cannot be predicted, you may use a unit upper bound on latency. That is, a message sent by a node reaches a neighbor in at most one unit of time. Also assume that tasks local to a node, including internal computations, and the sending and receiving of messages take negligible time. The time for the algorithm is the maximum time from the earliest point when at least one starting node is awake, to the point when the last starting node has gone back to sleep.

This question involves $k$-coloring the underlying graph $\mathcal{G}$. That is, assigning colors from a set $C_k = \{0, 1, \cdots, k-1\}$ to each node such that no two nodes of the same color have an edge between them.

In the following parts you must explain your algorithms from the point of view of nodes, indicating when the node wakes up, what it does while it is awake in response to an event, and when does it go back to sleep. You must justify all your answers.

(a)   Design a 2-coloring algorithm, if $\mathcal{G}$ is given to be a tree and if there is exactly one starting node. What is the time complexity of your algorithm. What is the message complexity of the algorithm (order of number of messages sent)? Recall that $n$, $m$, $\delta$ and $D$ denote the number of nodes, number of edges, degree and diameter of $\mathcal{G}$.

(b)   Let $\mathcal{G}$ be a general undirected graph. Design a $(\delta + 1)$-coloring algorithm assuming one starting node. What are is its time and message complexities?

(c)   What would change if there are multiple starting nodes that initiate the $k$-coloring algorithm in the previous two parts? How would you approach any problems caused by this?

   Given a region $S$ in the 2D plane, we say it is *convex* if and only if for any pair of points $p, q \in S$, the line segment $pq$ is completely contained in $S$. Let $P = \{p_1, p_2, \ldots, p_n\}$ be a set of 2D points. The *convex hull* of this point set $P$, $\mathcal{CH}(P)$, is the smallest *convex* set that contains $P$. For example, if $n = 2$, the convex hull of a point set $P = \{p_1, p_2\}$ with 2 distinct points is simply the line segment $p_1 p_2$.

   a) For a point set $P$ with 3 points, $n = 3$, what is the shape of $\mathcal{CH}(P)$? Discuss and illustrate all the possibilities. What about when $n = 4$?

   b) For a general point set $P$ with $n$ distinct points, one property of the convex hull $\mathcal{CH}(P)$ can be used for its computation. Consider a pair of points $p, q \in P$, if all the other points of $P$ lie either on or to one side of the straight line through $p, q$, then $pq$ is an edge of $\mathcal{CH}(P)$. Can you design an algorithm based on this to compute $\mathcal{CH}(P)$ for a given point set $P$? Elaborate how you represent and output the result. Analyze your algorithm's time complexity in big-O notation.

   c) Can you design an *incremental algorithm* to solve $\mathcal{CH}(P)$ in $O(n \log n)$ for a point set with $n$ points. An incremental algorithm means that you start with one point, and add the other points one by one, and update the resultant convex hull accordingly step by step. Analyze your algorithm and show why it is $O(n \log n)$.

Let $G = (T, E)$ be an undirected task graph, where $T$ corresponds to a set of tasks and an edge $(i, j) \in E$ if tasks $t_i$ and $t_j$ communicate. Each edge $(i, j)$ has a weight $c(i, j)$ denoting the volume of communication between $t_i$ and $t_j$. For an $m \times m$ mesh of cores, some tasks $P \subseteq T$ have been mapped to cores. Two arrays describe this mapping. Array *map_by_place*$(g, h) = i$ means that core $(g, h)$ has task $t_i$ mapped to it; *map_by_place*$(g, h) =$ NIL means $(g, h)$ is free. Array *map_by_task_ID*$(i) = (g, h)$ means that task $t_i$ has been mapped to core $(g, h)$; *map_by_task_ID*$(i)$ = NIL means $t_i$ has not been mapped.

(a) Design an algorithm to select the task in $T - P$ with largest communication volume to tasks in $P$.

(b) Design an algorithm to map the task selected in part (a) to a free core in $M$ such that overall communication cost is minimized. (For task $t_i$ mapped to core $(r, s)$ that communicates with task $t_j$ mapped to core $(g, h)$, the *communication cost* is $c(i, j) * [\,|\,r - g\,| + |\,s - h\,|\,]$. The overall communication cost for task $t_i$ is the sum of these communication costs between $t_i$ and all tasks in $P$ with which it communicates.)

(c) Derive the time complexity of the algorithms in parts (a) and (b). Let $n = |\,T\,|$, and let $q = |\,P\,|$.

Let $A = \langle a_1, a_2, \cdots, a_n \rangle$ be an array of $n$ numbers. For the purpose of the following definition, assume that $a_0 = a_{n+1} = -\infty$. Define array $A$ to be *positive unimodal* if and only if there is an index $1 \leq i \leq n$ such that $a_0 < a_1 < \cdots < a_{i-1} < a_i > a_{i+1} > \cdots > a_n > a_{n+1}$. A positive unimodal array has a unique local and global maximum. The array is *negative unimodal* if and only if the above conditions hold with $<, >$ exchanged and $a_0 = a_{n+1} = \infty$. A negative unimodal array has a unique global and local minimum. The array is *bimodal* if and only if there is an index $1 \leq j \leq n$ such that one of the two arrays $A_1 = \langle a_1, a_2, \cdots, a_j \rangle$ and $A_2 = \langle a_j, a_{j+1}, \cdots, a_n \rangle$ is positive unimodal and the other array is negative unimodal. A bimodal array has a local and global maximum and a local and global minimum.

Answer the following questions. All answers must be justified.

(a) Give an example of each of positive unimodal, negative unimodal and bimodal arrays.

(b) Let $A$ be an $n$ element positive unimodal array. Design a $O(\log n)$-time sequential algorithm to find the maximum element of $A$.

(c) Suppose you have a parallel system with $p$ processors and unrestricted access to shared memory (for accessing array $A$), how quickly can you solve the problem in part (b)?

(d) How would your answers to parts (b) and (c) change if $A$ was negative unimodal?

(e) How would your answers to parts (b) and (c) change if $A$ was bimodal?

Some online games have a set of servers $S$ such that a player can connect to any server. Say that a player is *satisfied* if he or she is connected to a server with delay at most $\Delta$. You are given a set $S$ of servers and a set $P$ of players such that array *assign*($j$) = $k$ means player $p_j$ is connected to server $s_k$. You are also given a delay matrix $D$ such that $D(j, k)$ is the delay between player $p_j$ and server $s_k$. Each server has capacity $c$; a server is *full* if it has $c$ players assigned to it.

When a player $p_g$ leaves the game from a full server $s_h$, then we can try to increase the number of satisfied players by the following algorithm. For each unsatisfied player (player with delay > $\Delta$), check if its delay to $s_h$ is at most $\Delta$, and if so, move the player to server $s_h$. Quit this algorithm when either moving an unsatisfied player to $s_h$ or after testing all unsatisfied players and discovering that no player will be satisfied by moving to $s_h$.

Attempt to improve this algorithm for increasing the number of satisfied players as follows.

(a) Describe an efficient data structure for each server $s_h$ that holds the set of unsatisfied players that would be satisfied if they were assigned to $s_h$.

(b) Describe an efficient algorithm using these data structures to attempt to increase the number of satisfied players when player $p_g$ leaves full server $s_h$.

(c) What is the time complexity of this algorithm? How much time does it take to update the data structures?

(d) Suppose a new player $p_{new}$ joins the game but receives an unsatisfying assignment. Describe how to update the data structures from part (a) and how much time this takes.

A set of $n$ stations share a channel that each processor could write to and read from. At any time the value read from the channel is the same for all stations and is called the *channel symbol*. For this problem, the channel symbol can take one of three values, $0, 1, \#$.

If no station writes to the channel, then the channel symbol is 0. If exactly one station writes to the channel then the channel symbol is 1; the value written by the station is not important. If more than one station writes to the channel, then the channel symbol is $\#$ (a special collision symbol).

This problem involves a MAC protocol, in which $Q$ "active" stations (where $2 \leq Q \leq n$) wish to acquire the channel. The active stations participate in a competition to win the channel; while the value of $Q$ is known to each active station, which other stations are active is is not known. At the end of the competition one active station is selected as leader and it acquires the channel. All other active stations are aware that they are not the leader. The stations select a leader using a randomized algorithm. The algorithm runs for several (potentially unbounded number of) rounds until a leader has been selected. The algorithm terminates once the leader has been selected. The following algorithm is executed in each round by each active station $i$ that wishes to acquire the channel.

```
/* Executed in parallel by all active stations i */
    Station i flips a coin with probability 1/Q of heads and probability 1 − 1/Q of tails
    Station i writes to the channel if and only if it flips heads
    Station i reads from the channel
    if the channel symbol is a 1 then
        if Station i wrote to the channel in the current round then
            Station i terminates as leader
        else Station i terminates as non-leader
        end_if_else
    end_if
```

Answer the following questions. All answers must be justified.

(a) Illustrate the algorithm for $Q = 2$ that terminates in 3 rounds, with channel symbols 0 and $\#$ in the first two rounds.

(b) For the general case of $Q$ stations wishing to acquire the channel, what is the probability that exactly one station will write to the channel?

(c) You are given that $\left(1 - \frac{1}{x}\right)^{x-1} > e^{-1} \approx 0.368$. Show that, on an average, the above algorithm terminates in a constant number of rounds (independent of $Q$).

(d) Indicate how you may approach the problem if each station did not know the value of $Q$.

A computer network organizes data in terms of transmission units such as frames or packets. In this problem we use the term "frame" in a general way to mean a transmission unit. Each frame has a payload (data to be transmitted) and an overhead (typically header information containing the identities of the source and/or destination, error codes etc.). For this problem, assume that the overhead is of fixed size and independent of the payload size. Also assume that the frame uses an error code that is capable of detecting any error and incapable of correcting any error.

Each transmitted bit has a probability of error $p$ (called the bit error rate or BER). A frame has an error if any one of its bits is in error. The larger the frame, the higher its probability of error. However, a small frame has higher overheads.

Answer the following questions. All answers must be justified.

(a)    If the BER is $p = 0.001$, then what is the probability that a 4-bit frame has an error.

(b)    If the BER is $p$, then derive an expression for $p_f$ the error probability of a frame with $h$ header bits and $b$ payload bits.

(c)    The underlying protocol demands that each erroneous frame be retransmitted until it is received correctly. For this question you need not consider the mechanism by which the sender determines if a frame has been correctly received. You can assume that the sender somehow knows to retransmit a frame when it has not been correctly received by the receiver.

Derive an expression, in terms of the frame error rate $p_f$, for the average number of times a frame must be transmitted.

(d)    If the objective is to reduce the total number of bits transmitted, how would you decide on the size of a frame?

(a) A denial-of-service attack involves loading a network resource to the point where it becomes non-functional.

(*i*) Explain how PING can be used to carry out a denial-of-service attack.

(*ii*) On October 21, 2002 the 13 DNS root servers were subject to a distributed denial-of-service attack. Explain the impact of the attack on the operation of the Internet if some of the servers are brought down; if all of the servers are brought down.

(b) Consider the following multi-point architecture, which consists of one primary (or host or front-end-processor) P and *N* equally spaced secondary terminals S$_i$.



Let $a$ = propagation time/transmission time, where the propagation time is from the primary to the farthest secondary. Assume *roll-call* polling. [*With roll call polling, terminals Si are polled in sequence by the front-end processor P. The front-end processor needs to wait for a response before the next terminal is polled. Terminals that have a message transmit it in response to the polling process. Terminals that do not have a message respond by sending a positive acknowledgement without any message.*] Also assume that the transmission time for the poll and that primary and secondary processing time are negligible and transmitted messages are of equal sizes. If every secondary is always ready to transmit a message, show that the line utilization is U = 1/(1+a). If only one station is ready to transmit during any polling cycle show that U = 1/(1 + a*N*).

Felix Baumgartner jumps from a plane; as he descends vertically down to earth, he takes photographs. At time instant $t_1$, a point from earth is imaged at pixel $(x_1, y_1)$; at time instant $t_2$, the same point appears at $(x_2, y_2)$. At time instant $t_2$, his altimeter shows that the distance to earth is $d$. (The focal length of the camera is $f$ and the pixel size is $\mu$.)

The view along the $y$ axis is shown below.
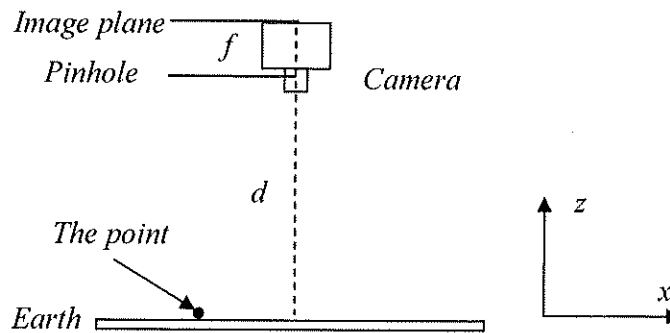


(a) What is the speed of Felix?

(b) How much time does Felix have before landing? (Assume he does not open his parachute and descends with constant speed.)

(c) The photographs Felix took look blurry due to his fast descent. He would like to restore the photographs by estimating the blur. Model the blur $h(x,y)$ in the photographs.

(State any assumptions you make in your solutions.)

Let $P = \{p_1, p_2, \ldots, p_n\}$ be a set of points in the plane. A *planar subdivision* of $P$ is a graph $G = \{V, E\}$ embedded in the plane, where $V = P$ and each edge $e = (p_i, p_j) \in E, p_i, p_j \in P$ is a straight line segment. A *maximal planar subdivision* $S$ of $P$ is a planar subdivision such that no new edge connecting two vertices can be added to $S$ without destroying its planarity, i.e., any edge that is not in $S$ intersects one of the existing edges. A *triangulation* of $P$ is a planar subdivision of $P$ where each bounded facet is a triangle. The left figure is a planar subdivision, and the right figure is a triangulation.
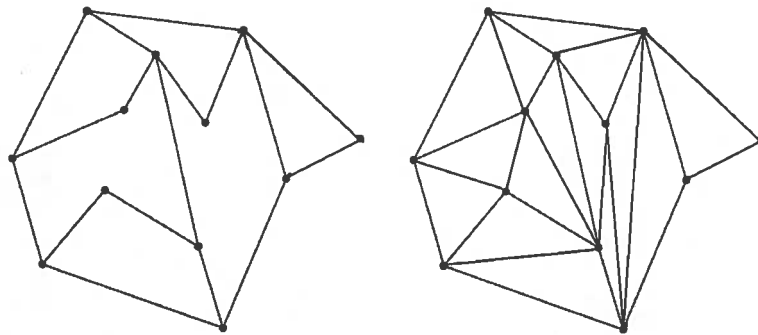


a) Prove that a maximal planar subdivision of $P$ is a triangulation.

b) Is a triangulation always a maximal planar subdivision? If so, prove it; if not, give a counter example.

c) Consider a convex polygon with $n$ vertices on its boundary, without introducing new interior point, one can construct a triangulation of this polygon. Does each triangulation scheme have the same number of triangles? If so, how many? If not, explain why.

d) Suppose an arbitrarily given polygon has $n$ vertices on the boundary and $m$ points inside the polygon; a triangulation that taking all these $n + m$ points as vertices can be constructed. Does each triangulation scheme have the same number of triangles? If so, how many? If not, explain and derive the number.

We have a setup consisting of (i) a point light source with radiance intensity $I$, located at $(x_s,y_s,z_s)$, (ii) a mirror with size $d$-by-$d$, located in the xz-plane, and (iii) a planar surface of infinite size, located in the xy-plane.

Note that $x_s = 0$ and $z_s < d$.
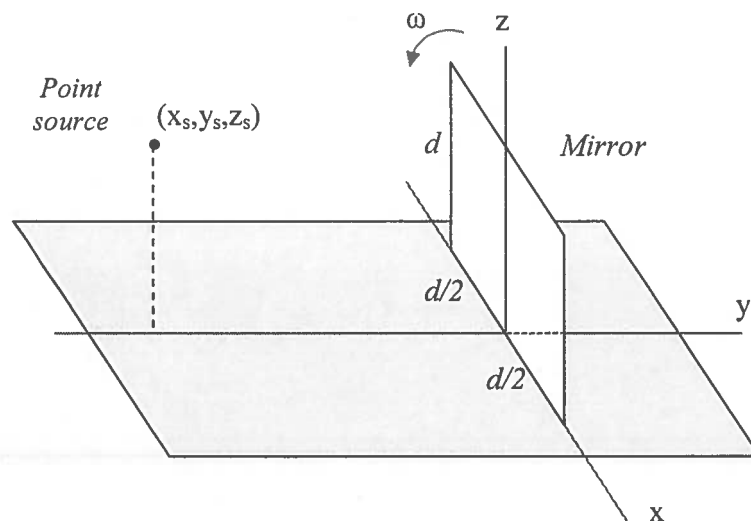


(a) What is the irradiance right below the point source?

(b) What is the irradiance at an arbitrary point on the surface?

(c) Suppose that the mirror starts to rotate along the x axis with an angular velocity of $\omega$ in the direction shown in the figure. Derive the irradiance right below the point source and plot it as a function of time.

(State any assumptions you make in your solutions.)

Quadric patches are 3D surfaces that can be represented implicitly as

$$S(x, y, z) = ax^2 + by^2 + cz^2 + dxy + eyz + fxz + gx + hy + jz + k = 0. \quad (1)$$

a) Many simple geometric primitives are in the family of quadric surfaces. Describe the coefficients of spheres, ellipsoids, cylinders, and planes.

b) Any quadric surface patch can be formulated using a matrix representation,
$$P^T Q P = 0,$$
where $P$ is a $4 \times 1$ vector and $Q$ is a $4 \times 4$ symmetric matrix. Derive $P$ and $Q$ from equation (1).

c) Given a 3D surface patch $S$, to compute its following geometric properties:

  (i) the normal of point $\mathbf{p}(x, y, z) \in S$ on the surface,

  (ii) whether a point $\mathbf{q}(x, y, z)$ is on $S$ or not,

  (iii) hidden surface determination through z-buffering, namely, given the $x$ and $y$ coordinates of a point $\mathbf{p} \in M$ on the surface $M$, to check $\mathbf{p}$'s depth coordinate $z$,

which representation scheme, triangle mesh or implicit quadric representation described above, is more efficient? You should elaborate your comparison on each of these three computations.

In the circuit below the field effect transistors have sharp thresholds of 2.5 Volts, and all the transistors may be considered ideal.

An sine wave at 1 kHz is applied to the input, centered at a dc voltage of 2.5 Volts with an amplitude of 1 Volt peak to peak.

a) With SW open, what is the input impedance?

b) With SW open, sketch the waveform at the output.

c) With SW closed, what is the input impedance?

d) With SW closed, sketch the waveform at the output.
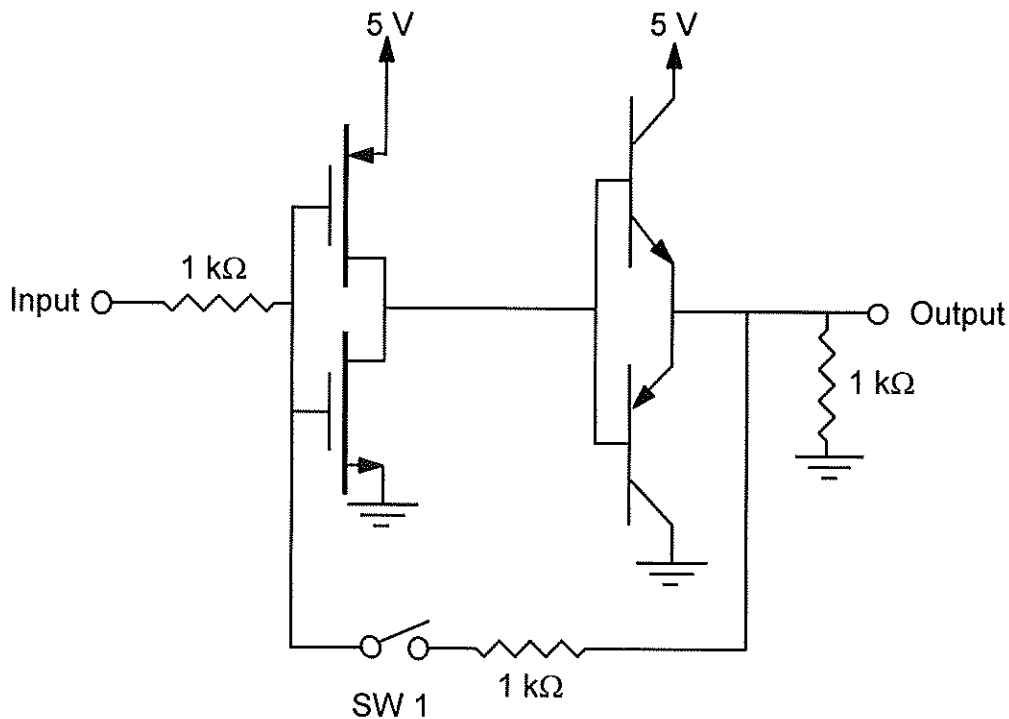
**Circuits and Systems**
**Problem 3**

For the amplifier circuit shown in the figure below,
a) Calculate the resistance values $R_{C1}$, $R_{C2}$, $R_{C3}$, $R_{C4}$, $R_{EE1}$ and $R_{EE2}$.
Given: $V_{CC} = +15V$, $V_{EE} = -15V$, Transistor base-emitter voltage during conduction $V_{BE(ON)} = 0.7V$.

For $Q_1$ and $Q_2$:
$I_{C1} = I_{C2} = 0.1$ mA
$V_{CB1} = V_{CB2} = V_{CC}/2$
$\beta_F = \beta_0 = 50$

For $Q_3$ and $Q_4$:
$I_{C3} = I_{C4} = 1$ mA
$V_{CB3} = V_{CB4} = (V_{CC}-V_{B3})/2$
$\beta_F = \beta_0 = 50$

Here, $\beta_0$ is d.c. common-emitter current gain and $\beta_F$ is forward small signal current gain. $V_{CBX}$ is the collector to base voltage and $V_{BX}$ is base voltage of transistor $Q_X$.
b) Calculate the above resistance values if the supply voltages are now reduced to that $V_{CC} = +6V$, $V_{EE} = -6V$.
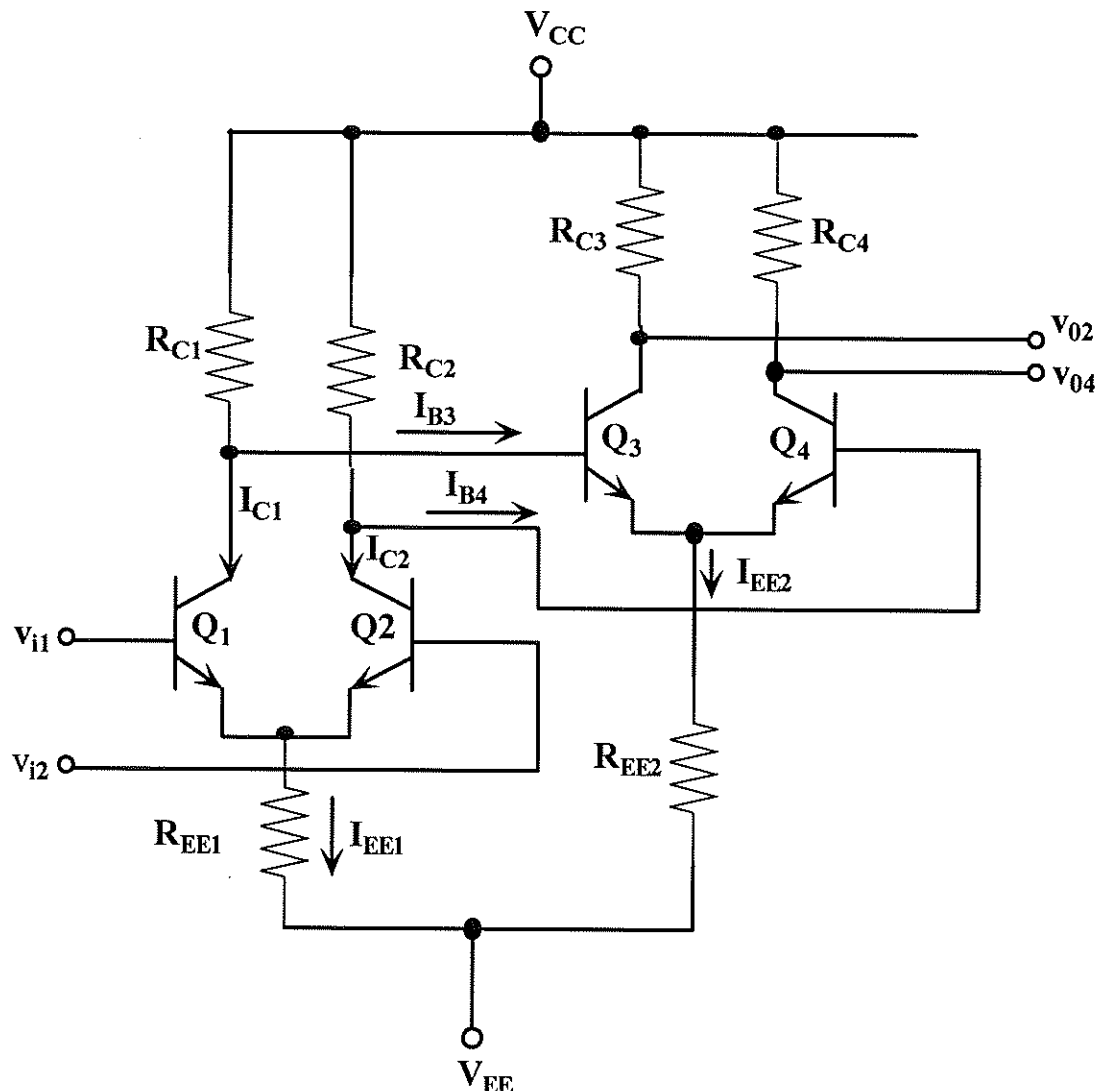
**Circuits and Systems**
**Problem 1**

Consider a bipolar junction transistor circuit shown below with $R_C = 2.2$ kΩ, $R_B = 22$ kΩ, $V_{BB} = 1.2$ V, and $V_{CC} = 12$ V. Assume $\beta = 100$, $V_f = 0.7$ V, and $V_{sat} = 0.2$ V for the transistor.
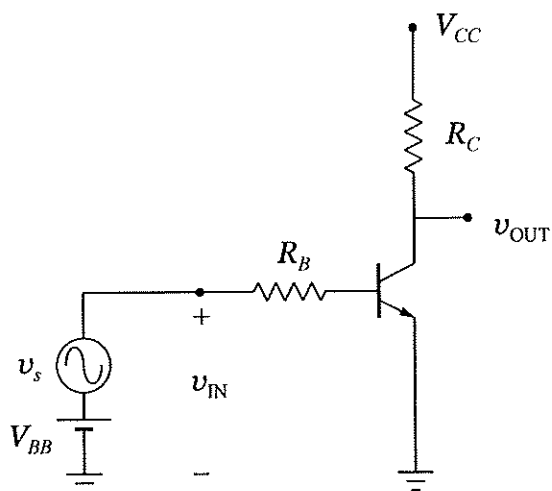


(a) Plot the transfer characteristic, $v_{OUT}$ versus $v_{IN}$, of the circuit.

(b) When $v_s = V_p \cdot \sin(2\pi f t)$, find the largest value for $V_p$ without the transistor going into saturation or cutoff regions. If needed, assume $f = 1$ kHz.

(c) Adjust $R_C$ and $R_B$ to double $V_p$ while maintaining the other conditions in (b). Then, present your opinion in detail whether this circuit would be better than the original circuit or not.

# Circuits and Systems
## Problem 2

a) In the circuit below $R_1$ = 100 k$\Omega$, $R_2$ is an open circuit, and $R_3$ = 1k$\Omega$. Find the voltage at the collector, $V_C$, if $\beta$ = 50 and -V is -10 Volts.

b) In the circuit below $R_2$ is again an open circuit, and $R_3$ = 0. No information is given about the other components. Find an expression for $\beta$ in terms of $V_A$ and $V_B$.

c) In the circuit below $R_1$ = $R_2$ = 100 k$\Omega$, $R_3$ = 1k$\Omega$, and $\beta$ = 50. Find the value of the voltage, -V, which maximizes the difference between $V_A$ and $V_B$.
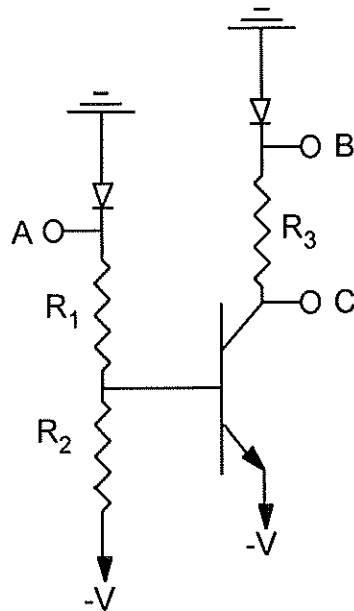
# Circuits and Systems
## Problem 3

In the circuit below both transistors have very high current gain, $\beta$. All the resistors are 1000 Ohms.

a) The output is a 1 Volt p-p square wave with a risetime T. Estimate the amplitude and rise time of the input.

b) Point A is connected to point B. Estimate the rise time of the output.

c) Point A is connected to point C. Estimate the rise time of the output.

d) Point A is connected to point D, making the circuit oscillate with no input. Estimate the frequency at which it oscillates.
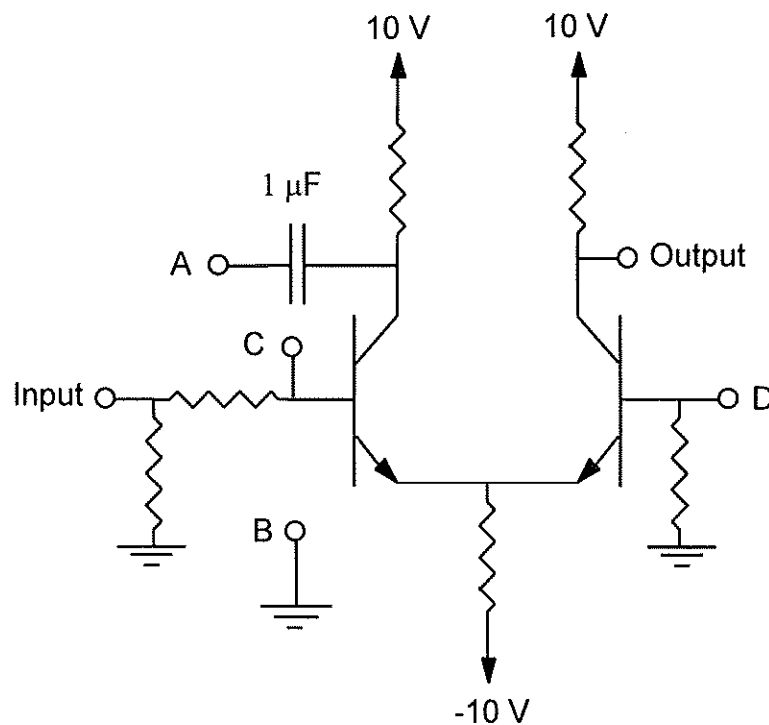
## Circuits & Systems
## Problem #4

The circuit shown in the following is a CMOS differential stage in which the aspect ratio W/L is indicated adjacent to devices. The NMOS devices have k = 25 $\mu A/V^2$, $V_T$ = 1.5 V, and $V_A$ (BJT equivalent Early voltage) = $1/\lambda$ = 100 V; the PMOS devices have k = 12.5 $\mu A/V^2$, $V_T$ = -1.5 V, and $V_A$ = $1/\lambda$ = 50 V.

Given:

$V_{GS8} = V_{DS8} = 3.45$ V

$I_D = [\{0.5\mu C_{OX}\}(W/L)(V_{GS}-V_{th})^2(1+\lambda V_{DS})]$

Where $\lambda$ is the channel length modulation parameter and k = $0.5\mu C_{OX}$. $I_D$ is the drain current, $\mu$ is the mobility of the carrier in the channel region, $V_{th}$ is the threshold voltage. $C_{ox}$ is the gate-oxide capacitance per unit area.

(a) Determine the bias currents in Q3, Q5, and Q7.

(b) Evaluate $|A_{DM}|$ and the CMRR.

(c) What will happen to CMRR if $1/\lambda$ of n-MOS current source is increased to 200V?
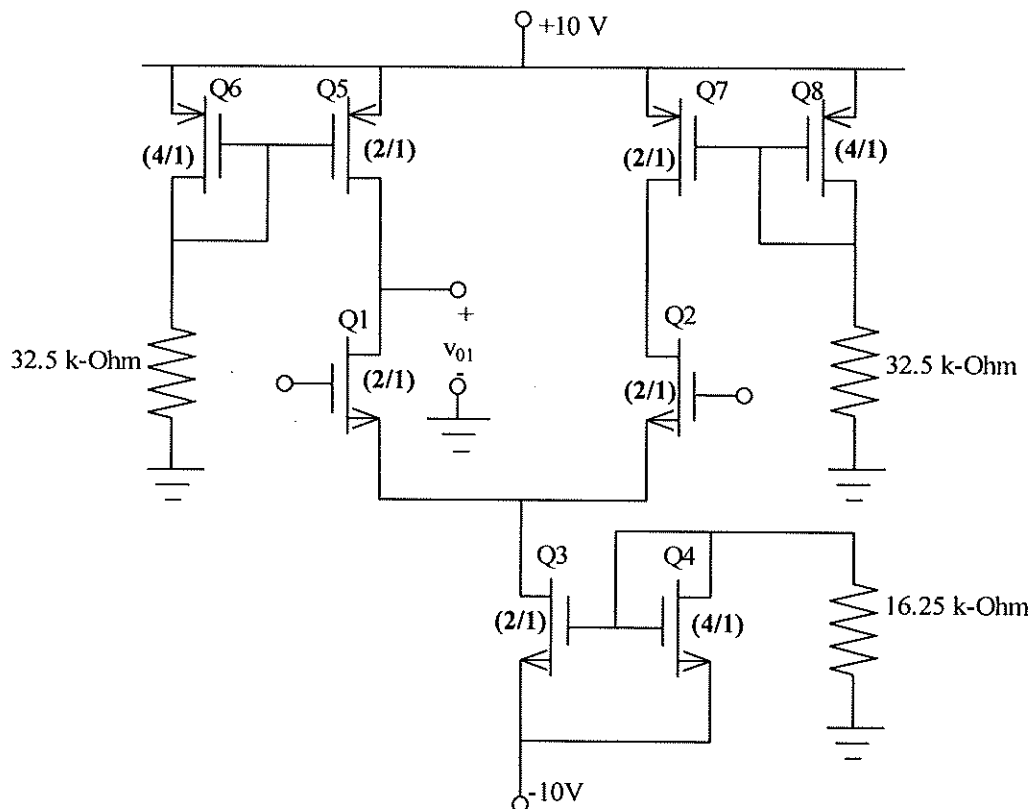
## Circuits & Systems
## Problem #5

Consider the following circuit. Device M1 is a standard NMOS device. Device M2 has all the same properties as M1, except that its device threshold voltage is *negative* and has a value of –0.4V. Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device M2 are the same as a regular NMOS. Assume that the input *IN* has a 0V to 2.5V swing. Note: Use SPICE MOS Model LEVEL 1 equations.
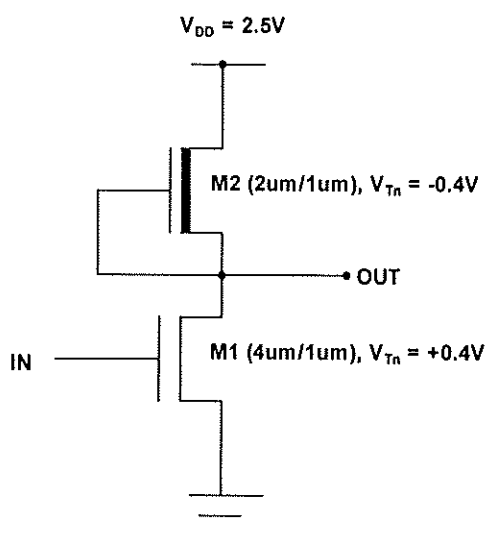


a) Device M2 has its gate terminal connected to its source terminal. If $V_{IN} = 0V$, what is the output voltage? In steady state, what is the mode of operation of device M2 for this input?

b) Compute the output voltage for $V_{IN} = 2.5V$. You assume that $V_{OUT}$ is small to simplify your calculation. In steady state, what is the mode of operation of device M2 for this input?

c) Assuming switching activity, $\text{Pr}_{(IN=0)} = 0.3$, what is the static power dissipation of this circuit? Use $V_{DS} = 0.63V$ in calculation.

**Given: SPICE MOS Model Level 1 Equations:**

$I_D = 0.5\mu C_{OX}(W/L)\{2(V_{GS}-V_{th})V_{DS}-V_{DS}^2\}$ (Linear region)
$I_D = 0.5\mu C_{OX}(W/L)\{(V_{GS}-V_{th})^2\}$ (Saturation region)
Where $V_{GS}$ is the gate-to-source voltage and $I_D$ is the drain current and
$\mu C_{OX} = KN$ (process transconductance parameter)

$KN_{M2}/KN_{M1} = 1$; $KN_{M2} = 115\mu A/V^2$

# Circuits and Systems
## Problem 2

1) In the circuit below the delay line is a cable, whose length is initially short compared to the rise time of the transistor, which has a high $\beta$. What is the voltage at the base of the transistor?

2) The length of the cable is increased until its delay is 1 microsecond, which is long compared to the risetime of the transistor. What is the frequency at which the circuit oscillates?

3) What is the amplitude of oscillation, as measured at the collector of the transistor?

5 V

1 kΩ

100 Ohm delay line

1 kΩ
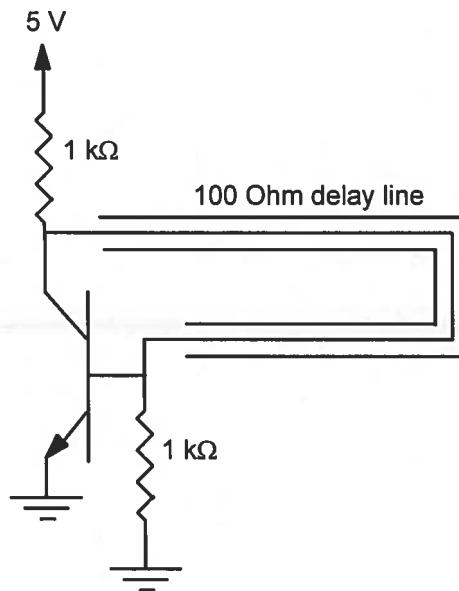
# Circuits and Systems
## Problem 3

Calculate the resistance of the following structures.

a. Calculate the resistance of a rod with a diameter of 100 um and a length of 1 mm. The resistivity is $\rho=0.5$ ohm·cm (You can assume that $\pi$ is equal to 3.)

b. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).
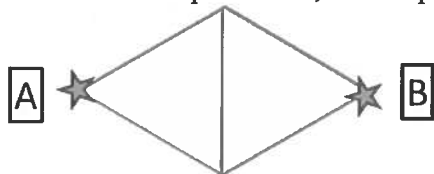


c. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).
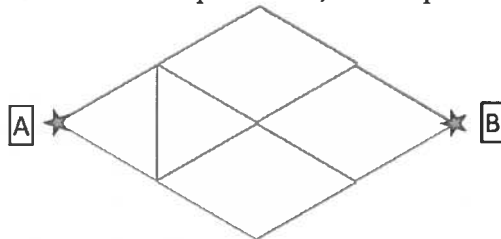


d. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).
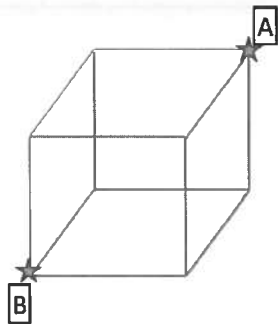


e. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).
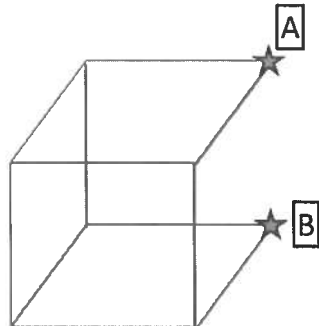
# Physical Electronics
## Problem 1

The energy E versus k relationship in a direct band gap compound semiconductor material (*material A*) for electrons in the valence band is given by $E = E_0 + A\cos ak$, where $E_0$, $A$ and $a$ are material constants and k is propagation constant (radians/m).

    a) Find the effective mass for valence band holes in this material at the top of the valence band i.e. band edge at $E = E_V$. Show intermediary steps.

    b) Current I = 1 mA flows through a bar made from p-type doped *material A* as shown in Fig. 1 below when $V_B = 5$ V.
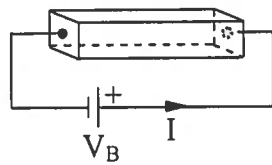


Fig. 1

        The composition of the material is slightly changed so that in this new semiconductor (*material B*), the E versus k relationship for electrons in the valence band is now given by: $E = E_0 + 2A\cos ka$. What will be the value of current I for this case if the bar in Fig. 1 is replaced by a bar made from *material B* having an identical size, shape and doping density? You may assume all other material properties to remain the same for these two materials. You must explain your answer clearly. State any assumptions made.

    c) Now assume that for *material B*, the mean free time between collisions for holes (relaxation time) decreases to 0.8 times its value in material A. Repeat part b) above for this case (i.e. find the new value of I for this case). You must explain your answer clearly.

## Physical Electronics
## Problem 2

A silicon n-channel MOSFET has substrate doping $N_A = 10^{16}$ cm$^{-3}$ and threshold voltage $V_T = 0.75$ V. The substrate is grounded. Both drain and source regions are heavily doped. Temperature $T = 300$ K.

a) Draw the cross-section of the MOSFET at the on-set of saturation showing all regions of the device. Carefully label your figure.

b) Determine the minimum channel length L (µm) so that the incremental change $\Delta L$ is no more than 0.1L (10 % of L) when drain to source voltage $V_{DS} = 5$ V and gate to source voltage $V_{GS} = 5$ V. Show intermediary steps and state any assumptions made. Explain your approach.

c) Will the value of L be smaller or larger or same compared to the case a) above if now $V_{GS} = 2$V keeping $V_{DS}$ constant at 5 V? Explain your answer giving reasons.

Depletion width W in a p-n junction is given by: $W = \sqrt{\dfrac{2\varepsilon_s}{q}\left(\dfrac{1}{N_A} + \dfrac{1}{N_D}\right)(V_{0bi} - V)}$   where

permittivity of Si $\varepsilon_s = 11.7\ \varepsilon_0$, permittivity of free space $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, magnitude of electron charge $q = 1.6 \times 10^{-19}$ C, $V_{0bi}$ is built in junction voltage and V is forward bias voltage applied to a diode. Boltzmann constant $k = 8.62 \times 10^{-5}$ eV/K, temperature $T = 300$ K, intrinsic carrier density in Si $n_i = 1.5 \times 10^{10}$ cm$^{-3}$ at 300 K, and Si band gap is 1.12 eV.

# Physical Electronics
## Problem 3

The lattice structure of a crystal is body-centered cubic (bcc). However, the Bravais lattice of this same crystal is a simple cubic (sc) structure.

a) For incident X-rays of wavelength ($\lambda$) equal to 1.542 Å, find the Bragg angles of X-rays scattered from the Bravais lattice of this crystal.

b) Find the primitive vectors ($\mathbf{b}_1$, $\mathbf{b}_2$, $\mathbf{b}_3$) of the reciprocal lattice for the sc lattice structure. The reciprocal lattice formula is as follows:

$$\mathbf{b}_1 = 2\pi \frac{\mathbf{a}_2 \times \mathbf{a}_3}{\mathbf{a}_1 \cdot (\mathbf{a}_2 \times \mathbf{a}_3)}$$

$$\mathbf{b}_2 = 2\pi \frac{\mathbf{a}_3 \times \mathbf{a}_1}{\mathbf{a}_1 \cdot (\mathbf{a}_2 \times \mathbf{a}_3)}$$

$$\mathbf{b}_3 = 2\pi \frac{\mathbf{a}_1 \times \mathbf{a}_2}{\mathbf{a}_1 \cdot (\mathbf{a}_2 \times \mathbf{a}_3)}$$

-where $\mathbf{b}_1$, $\mathbf{b}_2$, and $\mathbf{b}_3$ are the reciprocal lattice vectors corresponding to direct lattice vectors $\mathbf{a}_1$, $\mathbf{a}_2$, and $\mathbf{a}_3$.

c) Repeat part b) for the bcc lattice structure.

# Physical Electronics
## Problem 4

A coaxial capacitor consists of two conducting coaxial surfaces of radii $a$ and $b$ ($a<b$). The space between is filled with a dielectric material with dielectric constant $\varepsilon_r$.

(a) Use Gauss's law to calculate the capacitance per unit length.

(b) If the space between the two conducting surfaces is filled with two different dielectric materials with dielectric constants $\varepsilon_{r_1}$ for $0 < \phi < \pi$, and $\varepsilon_{r_2}$ for $\pi < \phi < 2\pi$ (see figure below), calculate the capacitance per unit length in two different ways:

i) Using Gauss's law.

ii) Using the fact that this configuration can be seen as two capacitors in parallel.

(c) Assuming that $b = 3a = 1.5$ cm , $\varepsilon_{r_1} = 2.3$, $\varepsilon_{r_2} = 5.4$, calculate the capacitance per unit length. (The free space permittivity is $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m .)
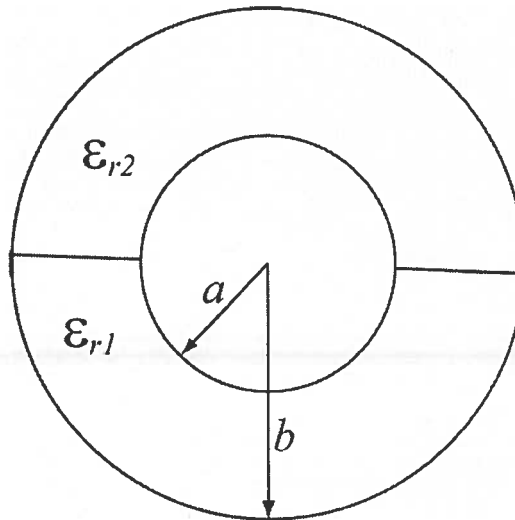
## Physical Electronics
## Problem 5

Consider a plane wave in free space with electric field $\mathbf{E}_i = \hat{x}E_0 \exp(-j\beta_0 z)$ ($\beta_0 = \omega\sqrt{\varepsilon_0\mu_0}$), which is normally incident on a dielectric slab of length $d$ and dielectric constant $\varepsilon = \varepsilon_r\varepsilon_0$ ($\varepsilon_r > 1$). The slab is bounded from a perfect electric conductor (PEC), which occupies the $z>d$ half-space. The electric field of the reflected wave for $z<0$ is $\mathbf{E}_r = \hat{x}RE_0 \exp(j\beta_0 z)$, where $R$ is the reflection coefficient. All fields have harmonic time dependence $\exp(j\omega t)$.

(a) Find the amplitude of the reflection coefficient $|R|$.

(b) Find the reflection coefficient $R$ when $\beta d = \pi$, where $\beta = \omega\sqrt{\varepsilon\mu_0}$.

(c) Find the reflection coefficient $R$ when $\beta d = \dfrac{\pi}{2}$.

(d) Find the surface current density at the interface between the slab and the PEC when $\beta d = \pi$.



$\mathbf{E}_i$    $\varepsilon_0$    Incident wave    $\varepsilon$    PEC    $d$    $z=0$    $z=d$    $X$    $Z$
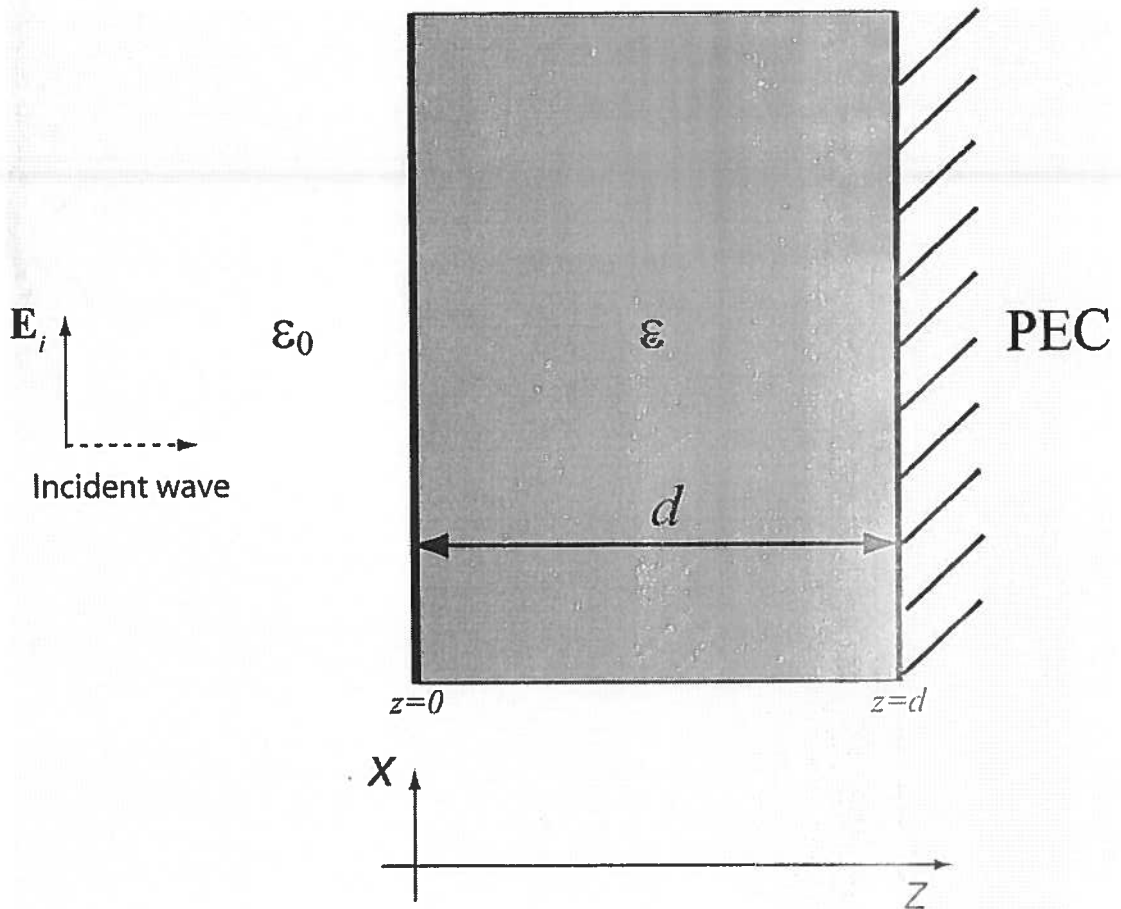
**Physical Electronics**
**Problem 1**

A silicon diode has the doping profile as shown in the figure below. $N_D$ and $N_A$ are donor concentration and acceptor concentration, respectively. Given,

$$p_0 = n_i \exp\left(\frac{E_i - E_F}{kT}\right) \text{ and } n_0 = n_i \exp\left(\frac{E_F - E_i}{kT}\right)$$

where $n_i$ is the intrinsic carrier concentration, $E_i$ is the intrinsic Fermi level, $E_F$ is the Fermi level, $k$ is the Boltzmann constant and $T$ is the temperature. $n_0$ and $p_0$ are electron and hole concentrations in equilibrium. $x_n$ and $x_p$ are $n$-side and $p$-side widths of the depletion region. Assume that $-x_p < -x_0$ for all applied biases of interest.

**Impurity concentration**
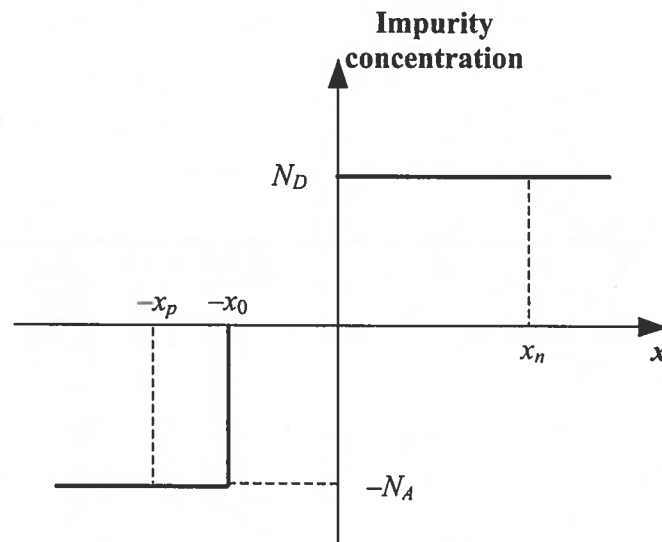


Given, $n_i = 1.45 \times 10^{10}$ cm$^{-3}$, $k = 1.38 \times 10^{-23}$ J/K, $T = 300$ K, $N_D = 5 \times 10^{15}$ cm$^{-3}$, $N_A = 1 \times 10^{16}$ cm$^{-3}$, and $x_0 = 0.5$ μm.

(a) Assuming impurities are 100% ionized, derive the expression for the built-in potential at thermal equilibrium. Justify your answer and show detailed steps.

(b) Calculate the built-in voltage ($V_{bi}$), $x_n$, and $x_p$.

(c) Draw an equilibrium band diagram.

(d) When a forward bias of 0.45 V is applied, repeat (b).

**Physical Electronics**
**Problem 3**

The figure below illustrates a semiconductor block for measuring the Hall effect. A current ($I$) is applied in $+y$ direction and a magnetic field ($B$) is applied in $+z$ direction. Answer the following questions.
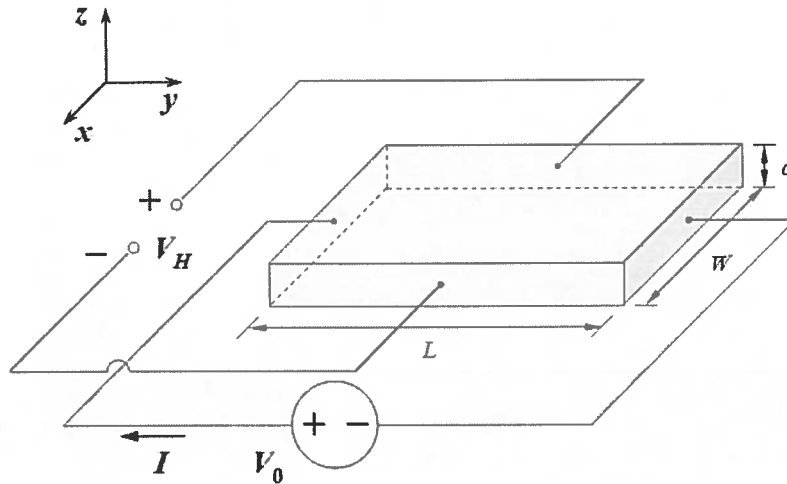


(a) Explain how the Hall effect can be used to distinguish the doping type of a semiconductor.

(b) Derive an expression of the Hall voltage $V_H$ for a $p$-type semiconductor. Define parameters if necessary.

(c) Consider that the silicon Hall sensor whose geometry is $L = 1$ mm, $W = 50$ μm, and $d = 5$ μm in the figure shown above is placed in the known magnetic field ($B$). When $B = 50$ mT (or 0.05 Wb/m$^2$), $I = 1$ mA, and $V_0 = 5$ V, the measured Hall voltage ($V_H$) is 5 mV. Determine the type, concentration, and mobility of the majority carrier.

(d) Will the Hall voltage have temperature dependence? Present your view on this.

1. The synchronous generator has the terminal voltage of 4 kV and it should be connected to the power line of 2 kV. What should be done to enable the generator to be connected to this line?
2. The nominal frequency of 3-phase synchronous generator is 50 Hz. What should be done in order to connect this generator to 3-phase system of the same nominal voltage but of 60 Hz frequency?
3. The electric energy should be send through the transmission line with the lowest power losses. What would you do to achieve this goal?
4. The induced phase voltage of 3-phase synchronous generator is distorted from sinusoidal shape and it contains the 3-d harmonic. The generator is connected to a 3-phase load. What would you do to make the 3-d harmonic of the current not to flow?

A. Develop power equation of the three-phase unbalanced linear-time invariant (LTI) load specified in terms of line-to-line admittances for harmonics $Y_{RS}$, $Y_{ST}$, $Y_{TR}$, assuming that the supply voltage is sinusoidal, but symmetrical and of the positive sequence.

B. Specify phenomena that affect the power factor of such loads.

C. Calculate the rms values of the active, reactive and unbalanced currents in the circuit shown in Figure and the power factor, $\lambda$, of the supply, assuming that $Z_R = 2+j3\ \Omega$.
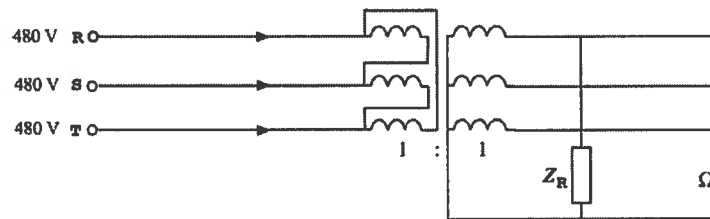
A Buck-Boost DC/DC converter supplied with voltage $U = 200$ V is used for the control of the output voltage on the resistance $R_0 = 15$ $\Omega$ from $U_1 = 100$ V to $U_2 = 300$ V. Draw the structure of the converter, the waveforms of the inductor and capacitor currents. Calculate inductance $L$ and capacitance $C$ of the converter if the switching frequency is equal to $f = 15$ kHz and output voltage ripples cannot be higher than 5 % of the output voltage.

1. Draw the equivalent circuit of a single-phase transformer. What kind of measurements have to be done to determine the parameters of this circuit?
2. Draw the phasor diagrams of currents and voltages, one for the inductive and one for pure resistive load. Show when the voltage regulation is greater.
3. A single phase transformer built (in Europe) for the rated frequency of 50 Hz is going to be connected to the power line (in US) of rated voltage and 60 Hz frequency. Will the power losses in the transformer increase or decrease with respect to those at 50 Hz frequency (assuming the transformer is loaded by the rated current in both circumstances). Explain what kind of power losses and why.
4. 3 single-phase transformers of the turn ratio 10:5 are connected to the 3 phase line of 220 V line voltage. Their primary and secondary windings are connected, first both in Δ and next both in Y.
   - Draw the circuit diagrams for both cases
   - What are the secondary phase voltage and the line voltage in each of the two connections?

1. Draw the equivalent circuit of the very long high voltage transmission lines. Draw its simplified equivalent circuit with a resistance, inductance, and capacitance.
2. Is there any limit of power transmitted by the line? Which of the line, resistive or inductive can transmit more maximum power?
3. How to minimize the voltage regulation (caused by the voltage drop along the transmission line) of the receiver? Is it possible to minimize it to zero? Explain how.
4. Draw the equivalent circuit of the inductive transmission line linking two systems. Using the voltage phasor diagram explain when the power can be transmitted from one system to another if the magnitudes of the voltages of both systems are equal.

Design a micro grid of PV rated at 200KW of power and at 230 V AC using a PV module with the following voltage and current characteristics. Determine the following:

a. Number of modules in a string for PV type 1
b. Number of strings in an array for PV type 1
c. Number of arrays
d. Inverter specifications
e. One-line diagram of the system

TABLE 5.47   Photovoltaic Module Data.

| Panel | Type 1 | Type 2 | Type 3 | Type 4 |
|---|---|---|---|---|
| Power (Max), W | 190 | 200 | 170 | 87 |
| Voltage at max. power point (MPP), V | 54.8 | 26.3 | 28.7 | 17.4 |
| Current at MPP, A | 3.47 | 7.6 | 5.93 | 5.02 |
| $V_{OC}$ (open-circuit voltage), V | 67.5 | 32.9 | 35.8 | 21.7 |
| $I_{SC}$ (short-circuit current, A | 3.75 | 8.1 | 6.62 | 5.34 |
| Efficiency | 16.40% | 13.10% | 16.80% | >16% |
| Cost | $870.00 | $695.00 | $550.00 | $397.00 |
| Width | 34.6" | 38.6" | 38.3" | 25.7" |
| Length | 51.9" | 58.5" | 63.8" | 39.6" |
| Thickness | 1.8" | 1.4" | 1.56" | 2.3" |
| Weight | 33.07 lbs | 39 lbs | 40.7 lbs | 18.3 lbs |

1- What is the maximum power transferable to the load?   (Assume a constant power factor – i.e. P/Q=constant and neglect R)

2- Draw a typical graph of load voltage vs. active power

3- Explain at least one method to overcome the voltage drop in case of high active power drop.
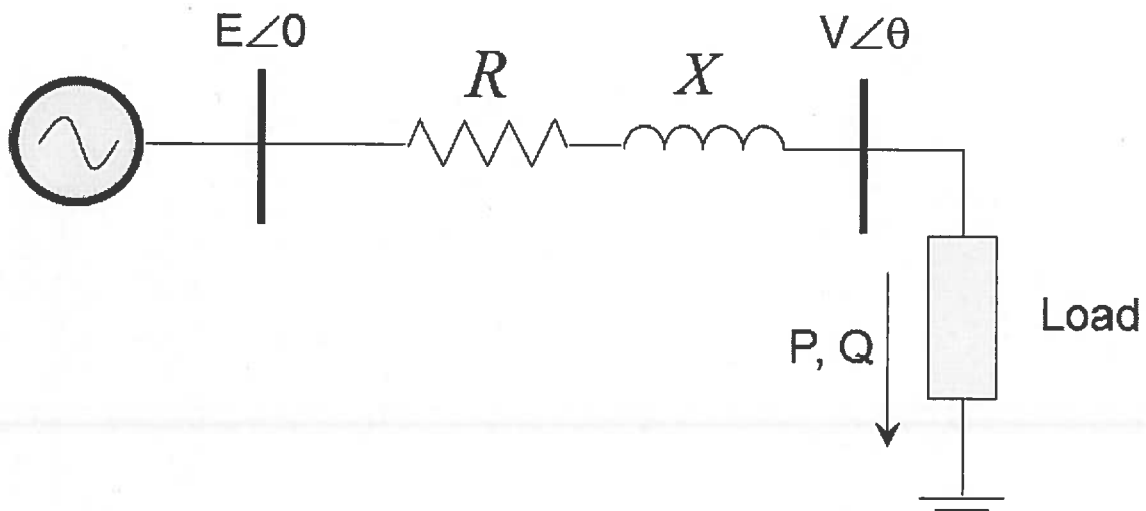
Consider open-loop transfer functions

$$L_1(s) = \frac{K(s-5)}{(s+5)(s^2+5s+6)}, \qquad L_2(s) = \frac{K(s+1)}{s^2(s+2)}.$$

(i) Sketch Bode diagram for $L_1(s)$ and Nyquist plot for $L_2(s)$.

(ii) Determine the stability range of $K$ for the closed-loop system with open-loop transfer function $L_1(s)$.

(iii) Determine the stability range of $K$ for the closed-loop system with open-loop transfer function $L_2(s)$.

Consider a linear system

$$\dot{x} = Ax + Bu, \quad y = Cx$$

with

$$A = \begin{bmatrix} A_1 & 0 \\ 0 & A_2 \end{bmatrix} \quad B = \begin{bmatrix} B_1 & 0 \\ B_3 & B_2 \end{bmatrix} \quad C = \begin{bmatrix} C_1 & C_2 \end{bmatrix}$$

(i) Give at least two methods for checking the controllability and observability for this system.

(ii) If $(A_i, B_i)$ are controllable for $i = 1, 2$. Is $(A, B)$ controllable? If it is, prove your conclusion using one of the methods you have described in the part (i). If it is not, give a counter example.

(ii) If $(A_i, C_i)$ are observable for $i = 1, 2$. Is $(A, C)$ observable? If it is, prove your conclusion using one of the methods you have described in the part (i). If it is not, give a counter example.

Verify if any of the following statements are correct. If yes, give a proof or justification. If not, give a counterexample or a proof.

1. $\dot{x} = Ax + bu_1$ is controllable if and only if $\dot{x} = Ax + bu_1 + Abu_2$ is controllable.

2. $\dot{x} = Ax + bu$ is controllable if $\dot{x} = Ax + Abu$ is controllable.

3. If $A$ is stable, then $\dot{x} = Ax + bu$ is controllable if and only if $\dot{x} = Ax + Abu$ is controllable.

4. If $A$ is stable, then $\dot{x} = Ax + bu$ is controllable.

Consider a unity negative feedback with an open loop transfer function

$$G(s) = \frac{20}{(s+1)(s+10)}$$

Design a controller so that steady state error respect to a unit ramp input is no more than 0.1 and settling time is no more than 1 second.

Let $G(s)$ be a transfer matrix

$$G(s) = \begin{bmatrix} \frac{1}{s(s+2)} & \frac{1}{s} \\ \frac{10}{s+2} & \frac{s}{s+1} \end{bmatrix}$$

(i) Find a minimal state space realizaiton.

(ii) Based on the state space realization in (i), find a state feedback control law so that the closed-loop poles are in $\{-1, -2, -3\}$.

(iii) Find a state observer so that the observer poles are at $\{-10, -10, -10\}$.

(iii) Find all transmission zeros of the transfer matrix.

Sketch root locus for

(i) $G(s) = \dfrac{s+2}{s(s+1)(s+3)(s+4)}$      (ii) $G(s) = \dfrac{s+4}{s(s+1)(s+2)(s+3)}$

and indicate the centroid, asymptotes, and $j\omega$-axis crossover frequency, if there is one.

Let $A$ be a real square matrix of dimension $n \times n$, $B$ of dimension $n \times 1$, and $C$ of dimension $1 \times n$. Consider the following Lyapunov equation:

$$AX + XA + BC = 0.$$

Assume that $\lambda_i(A) + \bar{\lambda}_k(A) \neq 0$ for all $(i, k)$. Show that the solution $X$ is nonsingular, if and only if $(A, B)$ is controllable and $(C, A)$ is observable.

Consider the following discrete-time linear and time-invariant (LTI) system

$$y[n] + y[n-1] - 12y[n-2] = x[n],$$

where $x[n]$ and $y[n]$ are, respectively, the input and output sequences.

1. Determine the frequency response of the above LTI system.

2. Determine the total solution for $n \geq 0$ of the above LTI system for an input $x[n] = 5\,\mu[n]$ and with the initial conditions $y[-1] = -1$ and $y[-2] = 1$. Here, $\mu[n] = 1$ for $n \geq 0$ and $0$ for $n < 0$.

COMMUNICATIONS AND SIGNAL PROCESSING 1

FALL 2013

The impulse responses of two discrete-time linear-time-invariant systems (filters) are given by $h[n]$, $g[n]$; their $z$-transforms are given by $H(z)$ and $G(z)$, respectively. Note that $h[n]$ and $g[n]$ can be *finite-impulse-response* (FIR) or *infinite-impulse-response* (IIR) systems. Also note that the frequency response of a lowpass filter is nonzero at zero digital frequency; the frequency response of a highpass filter is nonzero at the digital frequency of $\pm\pi$.

1. Suppose $h[n]$ is an FIR filter with filter length $N + 1$, i.e., $h[n] = 0$, for $n < 0$ and $n > N$, where $N$ is an arbitrary positive integer. If $h[n] = -h[N - n]$, for all $n$, show that $h[n]$ is never a lowpass filter.

2. Suppose $g[n]$ is an FIR filter with filter length $N+1$, i.e., $g[n] = 0$, for $n < 0$ and $n > N$, where $N$ is an arbitrary positive integer. If $g[n] = g[N - n]$, for all $n$, show that $g[n]$ is never a highpass filter.

3. If $G(z) = H(-z^{-1})$, determine $g[n]$ in terms of $h[n]$. If $H(z)$ is a highpass filter, show that $G(z)$ is a lowpass filter .

4. A lowpass filter $h[n]$ is an FIR filter with filter length $N + 1$, i.e., $h[n] = 0$, for $n < 0$ and $n > N$, where $N$ is an arbitrary positive integer. Assume that $G(z) = z^{-N}H(z^{-1})$. Determine $g[n]$ in terms of $h[n]$. Is $G(z)$ lowpass or highpass?

The unit-step input signal $u(n)$ is defined as 1 for $n \geq 0$ and 0 for $n < 0$. Consider a causal, linear and time-invariant (LTI) system whose input signal is given by $x(n) = u(n-1)$ and whose output signal is given by

$$y(n) = 2u(n) - (0.5)^n u(n).$$

1. Determine the impulse response $h(n)$ of this LTI system for all $n$ and justify all steps.

2. Determine whether the LTI system is memoryless or not.

3. Determine whether the LTI system is stable or not.

4. If the LTI system has the input signal $x(n) = (0.5)^n u(n) + u(-n)$, determine the corresponding output signal $y(n)$.

Assume that $\{X_n\}$ is a zero-mean, wide-sense stationary random sequence with autocorrelation function $R_X[k] = E[X_n X_{n+k}]$. The random sequence $\{Y_n\}$ is obtained from $\{X_n\}$ by $Y_n = \alpha^n X_n + X_{n-1}$, where $\alpha$ is a real-valued constant.

1. Find the autocorrelation function of $\{Y_n\}$.

2. Find the cross-correlation function of $\{X_n\}$ and $\{Y_n\}$.

3. Determine those values of $\alpha$ for which $\{Y_n\}$ is wide-sense stationary.

4. Determine those values of $\alpha$ for which $\{X_n\}$ and $\{Y_n\}$ are jointly wide-sense stationary.

A digital communication system with two equiprobable messages uses the following signals

$$s_1(t) = \begin{cases} 2 & 1 \leq t \leq 2 \\ 0 & \text{else} \end{cases}$$

$$s_2(t) = \begin{cases} -2 & 1 \leq t \leq 2 \\ 0 & \text{else} \end{cases}$$

1. Assume that the channel is additive white Gaussian noise (AWGN) with noise power spectral density of $N_0/2$. Determine the error probability of the optimal receiver.

2. Assume a two-path channel as shown in the following figure where $A = 1$. The noise processes $\{N_1(t)\}$ and $\{N_2(t)\}$ are independent white Gaussian noise processes each with power spectral density of $N_0/2$. The receiver receives both $r_1(t)$ and $r_2(t)$ and makes its decision regarding the message based on this observation. Find the structure of the optimal receiver and calculate its error probability.

3. Now suppose $A$ is a random variable which is uniformly distributed on the interval $[0, 1]$ and is independent of the message sequence and the noise process.. When message $m$ is transmitted, $r_2(t) = as_m(t) + N_2(t)$ is received where $a$ is the outcome of $A$. Suppose that the receiver knows the value of $a$.

   (a) What is the structure of the receiver in this case?

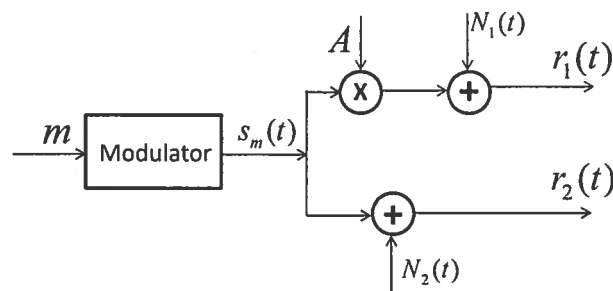   (b) Find the the average error probability of the receiver.



Figure 1:

In Figures 2 are two block diagrams illustrating the modulation and demodulation processes without directly using a sinusoidal signal $\cos(\omega_0 t)$.

Filters with impulse responses $h(t)$ and $g(t)$ are used at transmitter and receiver to produce $m(t)\cos(\omega_0 t)$, and $m(t)$, respectively. Here, $m(t)$ is the desired message signal whose bandwidth is $B$, i.e., its Fourier transform $M(j\omega) = 0$ for $|\omega| > B$, and $\omega_0 > 2B$ is the carrier frequency (See Figure 3).

The periodic signal $x(t)$ shown in Figure 3 has fundamental period $T_0 = \frac{2\pi}{\omega_0}$. In order to restore $m(t)$ at the output of $g(t)$, the following questions should be addressed in a sequel.

1. Compute the Fourier series $\{a_n, n = \cdots - 1, 0, 1, \cdots \}$, and Fourier transform of $x(t)$.

2. Determine the frequency response of the filter $h(t)$ so that its output is given by $r(t) = m(t)\cos(\omega_0 t)$.

3. Determine and draw the Fourier transform $Z(j\omega)$ of $z(t) = r(t)x(t)$.

4. Determine the Fourier transform $G(j\omega)$ of $g(t)$ to exactly restore $m(t)$ at the output of $g(t)$.
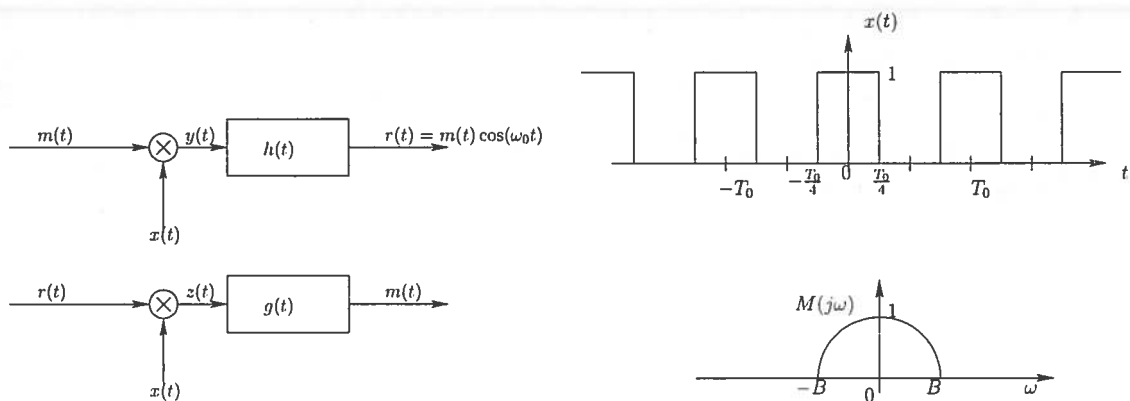


(a) Figure 2: Transmitter and Receiver Block Diagrams
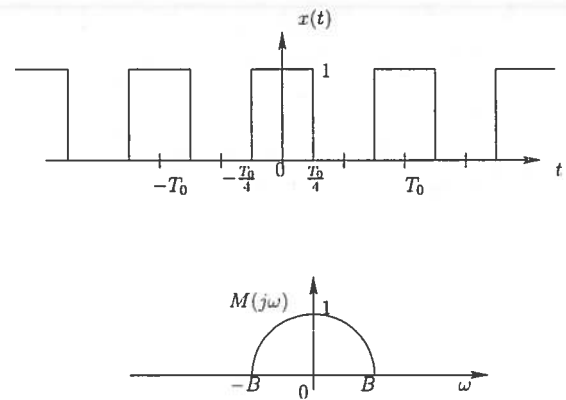


(b) Figure 3: Periodic Signal $x(t)$ and Fourier Transform $M(j\omega)$ of $m(t)$