MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

AUTOMATIC CONTROL TOPICS

A. Basic Tools

Laplace, Z transforms: basic properties, use in solving linear differential/difference equations, application to system analysis, transfer functions. Fourier transform, Fourier series: basic properties, application to signal analysis, frequency response, spectral energy density.

B. Basic Concepts

Linearity, time invariance, causality, difference and differential systems, linearization, signal-flow and block diagrams, BIBO and asymptotic stability.

C. Classical Control

Transient and steady state analysis and performance indicators, pole location, sensitivity; frequency domain analysis, phase and gain margins; Nyquist stability, Routh-Hourwitz criterion, root locus, lead and lag compensator design, PID control; pole placement with fractional controllers.

D. Sampled Data Systems

Basic A/D and D/A conversion, sampling theorem. Discretization of continuous time systems, deadbeat control.

E. State Space Control for Continuous and Discrete Time Systems

State and state equations, transition matrix, solution of state equation. Realization, controllability and stabilizability, observability and detectability, Lyapunov stability, state feedback and pole placement, asymptotic observers, state feedback with observers.

Representative References

1. C-T. Chen, *System and Signal Analysis*, Saunders College Publishing.
2. B.C. Kuo, *Automatic Control Systems*, Prentice Hall.
3. G.F. Franklin, J.D. Powell, A. Emami-Naeini, *Feedback Control of Linear Systems*, Addison Wesley.
4. G.F. Franklin, J.D. Powell, M.L. Workman, *Digital Control of Dynamic Systems,* Addison Wesley.
5. K. Ogata, *Discrete-time Control Systems*, Prentice Hall.
6. W.L. Brogan, *Modern Control Theory*, Quantum Publishers, Inc.
7. T. Kailath, *Linear Systems,* Prentice Hall.
8. K. Ogata, *Modern Control Engineering*, Prentice Hall.
9. C. T. Chen, *Linear system Theory and Design*, 3rd Ed., Oxford University Press, 1999.

M.S. Comprehensive /Ph.D. Qualifying Exam

Communication and Signal Processing Topics

Probability Theory and Random Processes
Basic concepts in probability theory; stationarity and wide sense stationarity of random processes, power spectral density, linear filtering of random processes, minimum mean squared error estimation, Gaussian and Poisson random processes.

Signals, Systems, and Digital Signal Processing
Continuous time and discrete time signals and systems: fundamental concepts, system properties (causality, stability, time invariance, etc.); time and frequency domain characterization of discrete and continuous time signals and systems; transform domain techniques; sampling and reconstruction; sampling rate conversion, frequency-domain analysis, aliasing and Nyquist rate concepts; discrete Fourier Transform and FFT algorithms; design and implementation of FIR and IIR filters.

Analog Communication
Amplitude modulation techniques; frequency and phase modulation techniques; sampling, quantization; pulse code modulation (PCM); effect of noise on continuous wave and PCM systems.

Digital Communication
Signal space representation; baseband representation of bandpass signals and systems; maximum likelihood (ML) detection and estimation; optimum receiver principles. performance of optimum receivers; differential, partially coherent and non-coherent detection of signals; bandwidth efficiency and power efficiency; receiver design and performance analysis of digital modulation schemes in fading channels; linear block codes and their decoding strategies, hard decision and soft decision decoding.

Representative References

1. Simon Haykin, *Communications Systems*, (Wiley).
2. J. G. Proakis and M. Salehi, *Communication Systems Engineering, 2nd Edition*, Prentice Hall.
3. J. G. Proakis, *Digital Communication*, 4th Edition, McGraw-Hill, 2000.
4. J. M. Wopzencraft and I. M. Jacobs, *Principles of Communication Engineering*, John Wiley & Sons, New York, 1965.
5. Henry Stark and John W. Woods, *Probability and Random Processes with Applications to Signal Processing, 3rd Edition.* Prentice-Hall.
6. *Probability, Random Variables, and Stochastic Processes*, A. Papoulis, 3rd edition, McGraw-Hill, 1991.
7. S. K. Mitra, *Digital Signal Processing*, 3rd edition, McGraw-Hill.
8. A. V. Oppenheim and R.W. Schafer, *Discrete-time Signal Processing*, Prentice-Hall.

MS COMPREHENSIVE / PHD QUALIFYING EXAM

COMPUTER ENGINEERING TOPICS

Appearing below is an outline of topics which computer-area questions will be based on. Most of the topics clearly fall into one of the three question areas, Hardware, Software, and Applications, but questions in one area can draw on topics from other areas. For example, the solution to an algorithm (software) question might require knowledge of cache organization (hardware).

Topics described with "Proficiency in" (or similar wording) must be understood very well, as though you were going to take a test in a course covering the topic. Topics described using "Competence with" (or similar wording) must be understood well enough to solve problems or answer substantive questions, however definitions or other background might be provided as part of the question. This information should help students that know the material make a quick start solving the problem. For topics listed under "Familiarity with" students should have a basic background in the area, including basic terminology, but need not know many specifics. For these problems a greater amount of background will be provided, enough so that a good student might be able to solve them without having taken any courses covering the topic.

Logic Design

Proficiency with combinational and sequential logic theory at EE 2720 and EE 2730 level, including Boolean algebra and basic minimization techniques. Proficiency in designing basic combinational and sequential circuits.

Computer Arithmetic

Proficiency with signed integer representations and with full adder and carry look-ahead adder designs. Competence with basic integer multiplication and division circuits. Competence with floating-point (FP) representations, including IEEE 754, and with FP arithmetic. Familiarity with modular and residue arithmetic.

Computer Instruction-Set Architecture (ISA) and Microarchitecture

Proficiency with 5-staged pipelined RISC (e.g., MIPS) implementations, including design rationale, direct and bypassed data paths, control signals, and relationship between implementation and instructions. Competence in assembly language programming, including RISC instruction sets. Competence with instruction set design issues, including memory addressing modes, and the variety of jumps & branch instructions. Familiarity with interrupts, traps, and exceptions. Familiarity with pipeline depth and superscalar width issues. Familiarity with caches and branch prediction techniques.

Computer Communication Networks

Competence with basic switching and multiplexing techniques. Familiarity with network layers and protocol stacks, ARQ protocols, error detection and correction. Familiarity with Internet addressing and routing standards and techniques. Familiarity with network reliability, availability, structural reliability terminology and techniques.

Algorithms and Data Structures

Proficiency with basic data structures (including arrays, stacks, linked lists, trees), basic algorithms (including binary search, merge sort, tree searches), memory content and layout of numbers, pointers, arrays, and structures complexity analysis of algorithms. Competence with advanced data structures (including hash tables, graph representations), algorithmic paradigms (including divide and-conquer, greedy, dynamic programming) and analysis techniques (including recurrence relations, amortized analysis). Familiarity with computational complexity and intractability randomized, online and approximation algorithms.

Parallel and Distributed Computing

Competence in major parallel system organization topics including hardware organizations (CPU & network), parallel program organizations (processes, tasks, or threads), communication models (message passing or shared memory). Competence with metrics for analysis of performance including speedup, efficiency, time complexity, and space complexity. Competence with use and implementation of basic synchronization primitives and constructs including compare & swap, atomic memory operations, semaphores, and barriers. Competence with basic parallel algorithms including reduction, sorting, leader election, graph algs, etc. Competence with common interconnects including bus, crossbar, mesh, hypercube networks.

Familiarity with other interconnects including Log n stage networks (e.g., omega), Clos and Benes networks.

Operating Systems and Compilers

Competence with coordination concepts, constructs, and issues, including multiple-process access to shared structures, mutual exclusion, and deadlock. (See also basic synchronization topics under Parallel and distributed computing.) Competence with basic memory management issues including virtual and physical addresses and their rationale virtual to physical address translation techniques, page swapping basics. Competence with program compilation techniques, including control-flow and data-flow program representations, dependencies and dependence testing, common optimizations, and common program transformations.

Computer Vision and Image Processing

Proficiency in geometric and radiometric image formation. Proficiency in image segmentation, enhancement and restoration techniques. Competence in image compression and morphological image processing. Familiarity with pattern recognition techniques.

Logic Testing and Reliability

Familiarity with fault models, including the stuck-at model.

MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

ELECTRONICS ENGINEERING TOPICS

A. Circuits

Circuit applications of diodes. Circuit applications of BJT, MOSFETs and JFETs in linear and digital circuits. Linear applications include amplifiers, oscillators, differential amplifiers and operational amplifiers. Applications of ideal operational amplifiers. Digital applications include internal operation of standard logic gates used as building blocks in logic families such as TTL, ECL, NMOS and CMOS.

B. Devices

Basics of carrier transport in semiconductor materials, physics of p-n junction diodes, bipolar and field effect transistors. Derivation of terminal current-voltage characteristics of discrete devices, large and small signal models. Basic physics of photonic devices. Basic integrated circuit technology.

C. Fields

Static fields, Maxwell's equations, propagation through istropic medium, reflections and basic antenna theory.

Representative References

1. M.N. Horenstein, *Microelectronic Circuit and Devices*, Prentice Hall.
2. Mitchell & Mitchell, *Introduction to Electronic Design*, 2nd Ed., Prentice Hall.
3. Gray & Mayer, *Analysis and Design of Analog Integrated Circuits*, 3rd Ed., John Wiley.
4. D. A. Hodges, H. G. Jackson and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, 3rd Ed., McGraw-Hill.
5. B. Streetman, *Solid State Electronic Devices*, 3rd Ed., Prentice Hall.
6. J.P. McKelvey, *Solid State and Semiconductor Physics*, Harper & Row.
7. Shen, *Applied Electromagnetics*, 2nd Ed., Prindle-Weber-Schmidt.

COMPREHENSIVE MS/QUALIFYING PH.D. EXAM

POWER ENGINEERING TOPICS

A. Electric Machinery

Maxwell's equations; analysis of simple electromechanical devices using Maxwell's equations; synchronous machines, voltage behind reactance model, Park transformation, d,q equations; exact and approximate equivalent circuits of single-phase transformers, nonlinear effects; modeling and calculation of its parameters of transmission lines; modeling and analysis of direct current and induction machines.

B. Power Systems

Per-unit calculations; symmetrical components; sequence impedances of transformers, synchronous machines and induction motors, sequence impedances and capacitances of transmission lines; sequence networks for fault analysis; shunt faults (3-phase, LG, LLG, LL faults); series faults (1LO, 2LO); power flow equations, (Decoupled) Newton-Raphson, Gauss/Gauss-Seidel methods; optimal dispatch with/without line losses; transient stability, swing equation, equal area criterion, effect of clearing time; low-frequency oscillations, supplementary excitation/governor control; linear optimal stabilization.

C. Power Electronics

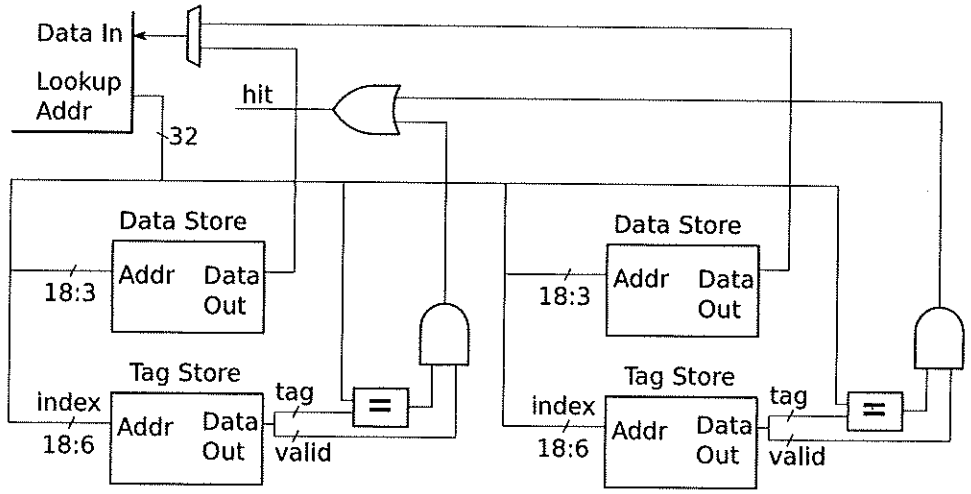
Fourier series of nonsinusoidal voltages and currents; analysis of circuits with nonsinusoidal voltage and current waveforms, nonsinusoidal active and apparent powers; single-phase and three-phase rectifiers, controlled AC/DC converters, DC/DC converters, inverters.

Representative References

1. R.D. Schultz & R.A. Smith, *Introduction to Electric Power Engineering,* John Wiley, 1988.
2. V. DelToro, *Electric Power Systems*, Prentice Hall, 1992.
3. P.M. Andersen, *Analysis of Faulted Power Systems*, The Iowa State Univ. Press, 1983.
4. Y.N. Yu, *Electric Power System Dynamics*, Academic Press, 1983.
5. M.H. Rashid, *Power Electronics*, Prentice Hall, 1988.
6. N. Mohan, T.M. Undeland, W.P. Robbins, *Power Electronics*, John Wiley, 1989.

The code fragment below runs on an ordinary 1 MiB two-way set-associative cache with 64-byte lines and using LRU replacement. The cache is partly illustrated below. For the questions below assume that the cache is empty when the code starts to run.

```
// Note: sizeof(a[0]) = 4.
const int stride = 1 << 20;
for ( int j=0; j<stride; j++ )
  for ( int i=0; i<32; i++ )
    sum += a[ i * stride + j ];
```



(*a*) Find the cache hit ratio due to accesses to a (see last line of code fragment above).

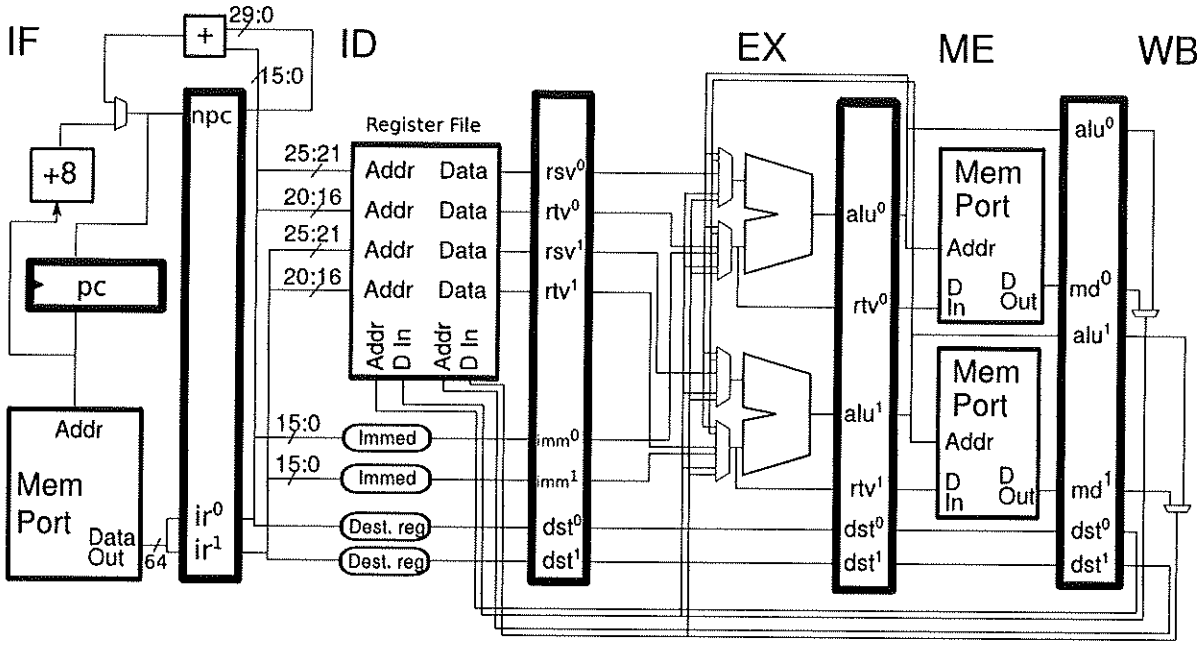
The index (address used for the tag store, see lower part of diagram) in this ordinary cache is a bit range, bits 18 downto 6, of the lookup address. This is fast and cheap, but it results in poor performance of the code above.

(*b*) Find an alternative way of computing the index such that the code above and also the code below run with the maximum possible hit ratio. The index must still be computed in terms of the lookup address. Show the logic for computing the index and any other changes needed.

```
for ( int i=0; i<2; i++ )
 for ( int j=0; j<some_limit; j++ )
     sum += a[ j ];
```

(*c*) Find a method of computing the index that will avoid conflict misses (which is what the code in the first part suffers from) for any power of two stride. Prove your answer.

Consider the execution of the code fragment below on the 2-way superscalar statically scheduled five-stage MIPS implementation illustrated below.




```
addi r7, r8, 1   IF ID EX ME WB
sub  r6, r7, r1  IF ID -> EX ME WB
```

Notice that execution stalls due to a dependence between the `addi` and `sub` instructions.

Consider an alternative design to avoid the stall. Design E1M1 has one ALU in the `EX` stage and one in the `ME` stage.

(*a*) Show where the two ALUs should be placed in the E1M1 design.

- Provide sufficient connections so that the code above runs without a stall.
- Sketch enough of the original design to provide context for the ALU placement.

(*b*) Compare the cost of bypass hardware on the E1M1 design and the original design, ignoring issues related to the `ME`-stage memory ports. Quantify the cost in a reasonable way.

(*c*) Provide a code fragment that will run *more slowly* on the E1M1 design than on the original design. Use pipeline execution diagrams for the two systems to illustrate the performance difference.

(*d*) Is E1M1 better or worse than the original design? Assume that a compiler will properly target code for each. Argue in terms of how fast code executes (referring to answers above and perhaps additional code fragments), the cost difference between the two, and anything else that is relevant.

Provide a brief argument, referring to answers above.

Computer Hardware 3 Fall 2012

A chip-multiprocessor (CMP) includes on one chip at least two processor cores, each with their own L1 cache; in an L2P CMP each core also has its own L2 cache and in an L2S CMP the cores share a single L2 cache. The figures for L2S and L2P CMP are shown as follows.

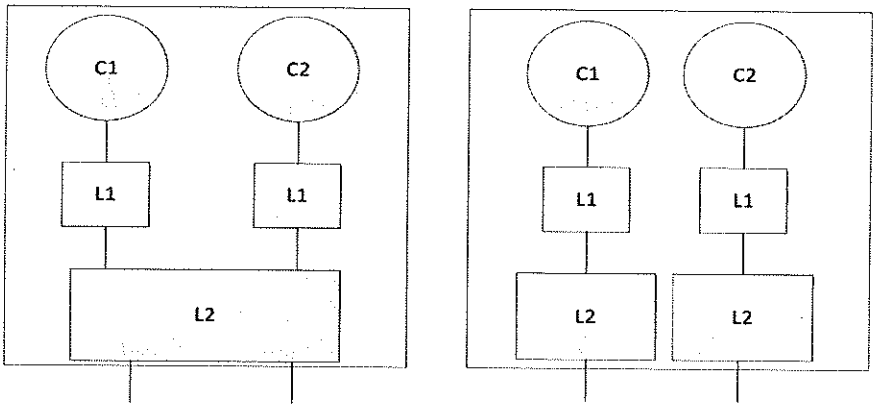


Figure. (a) Shared L2 cache; Figure (b) Private L2 cache.

A. Describe major advantages and disadvantages of having a shared L2 cache in comparison with a private L2 for each processor. You should answer the question with respect to the cache size, the access time and the cache coherence differences taking into account realistic implementation issues.

B. For a dual core processor, consider an L2P with two private 1 MB L2 caches (2 MB total on chip) and an L2S with a shared 2 MB L2 cache. Write two programs to illustrate the advantages and disadvantages. One program must run better on the shared L2 and the other program must run better on the private L2.

Computer Hardware 4 — Fall 2012

Single-event upsets from particle strikes have become a key challenge in processor design. The shrinking processor feature size, lower threshold voltage and increasing clock frequency make modern processors highly vulnerable to transient faults. Architectural Vulnerability Factor (AVF) reflects the possibility that a transient fault eventually causes a visible error in the program output, and it indicates a system's susceptibility to transient faults. To estimate the AVF, architects track the subset of processor state bits required for architecturally correct execution (ACE). Any fault in a storage cell that contains one of these bits, which we call ACE bits, will cause a visible error in the final output of a program in the absence of error correction techniques. We call the remaining processor state bits un-ACE bits, as their specific values are unnecessary for architecturally correct execution. A fault that affects only un-ACE bits will not cause an error. The AVF of a hardware structure is defined as follows.

$$AVF = \frac{\sum \text{residency (in cycles) of all ACE bits in a structure}}{\text{total number of bits in the hardware structure} \times \text{total execution cycles}}$$

A. In a 32-bit out-of-order pipelined processor whose instruction format list as follows. Rd is the destination register while Rs and Rt are two source registers. In case that only one source register is used, the Rt field remains as all "0".

Opcode (17 bits)	Rd (5 bits)	Rs (5 bits)	Rt (5 bits)

According to the above definition, what's the AVF for the following components or instructions: (1) branch predictor; (2) the program counter register; (3) mispredicted instructions; (4) NOP instruction in an instruction queue entry; (5) Dynamically dead instructions whose destination registers are not used. (6) Empty reorder buffer (ROB) entries. Justify your answer.

B. In the processor described as part (A), the ROB has 6 entries with each has 70 bits which include the encoding bits of instructions and other bits such as program counter, status of the instruction (issued, completed, etc). The following program has been loaded into the ROB at the beginning of cycle 0.

```
        SUBUI   R3, R1, #2
        BNE     R3, L1
        ADDUI   R1, R0, #3
L1:     SUBUI   R3, R2, #2
        SUBUI   R1, R2, #5
        ADD     R3, R1, R0
```

Right after cycle 2, the BNE instruction was found mispredicted. Therefore, the ADDUI instruction was squashed. Then the program only has five instructions remaining in the ROB. This means that there is an empty ROB entry starting from this point. All instructions finish and are flushed at the end of cycle 10. Calculate the AVF of this program. Justify your answer.

Let undirected graphs $\mathcal{G}_1 = (V_1, E_1)$ and $\mathcal{G}_2 = (V_2, E_2)$ represent interconnection networks for a systems with node sets V_1 and V_2. Except in the last part of this question, we will assume that $|V_1| = |V_2|$; that is, both graphs have the same number of nodes.

An *embedding* of $\mathcal{G}_1$ in $\mathcal{G}_2$ is a bijection $f : V_1 \longrightarrow V_2$ (a mapping of each node of $\mathcal{G}_1$ to a unique node of $\mathcal{G}_2$). This implicitly maps each edge $(u, v) \in E_1$ to a path in $\mathcal{G}_2$ between $f(u)$ and $f(v)$. Let this path be a minimum length path. Let P_2 be the set of paths in $\mathcal{G}_2$ to which edges of $\mathcal{G}_1$ are mapped.

The *dilation* of the embedding f is defined to be $\max\{\text{length of path } p \ : \ p \in P_2\}$ (that is, the length of the longest path that any edge of $\mathcal{G}_1$ is mapped to).

(a) An n-node ring is a graph with nodes $0, 1, \cdots, n-1$ and edges (i, j), where $0 \leq i < n$ and $j = (i+1) (\text{mod } n)$. An n-node linear array is a graph with nodes $0, 1, \cdots, n-1$ and edges $(i, i+1)$ for $0 \leq i < n-1$. The linear array does not have the edge $(n-1, 0)$ that is present in the ring.

Show that there is a dilation-2 embedding of a 5-node ring in a 5-node linear array.

(b) An $x \times y$ mesh is an x-row, y-column two dimensional array of nodes with each node connected to its four neighbors to the top, bottom, left and right. It is an extension of a linear array to two dimensions.

A similar extension of a ring to two dimensions results in a torus, which is a mesh with additional "wrap-around connections" between the first and last node of each row and each column.

Show that there is a dilation-2 embedding of an $x \times y$ torus in an $x \times y$ mesh.

(c) Graph embedding is also possible among graphs with different number of nodes; that is, $|V_1| \neq |V_2|$. Here f is no longer a bijection. The definition of dilation is unchanged, however.

Show that for sufficiently large n, there exists no dilation-1 embedding of an n-node balanced binary tree in an $n \times n$ mesh.

Suppose that three of your friends have decided to hike from Baton Rouge to International Falls, Minnesota next summer. They want to hike this trail in as few days as possible, but do not want to hike after dark. They have identified a large set of good *stopping points* for camping, and they will use the following scheme to decide where to camp. Each time they reach a possible stopping point, they check whether they can make it to the next one before the sun sets. If they can make it, then they keep hiking; otherwise, they stop.

More formally, model the trail from Baton Rouge to International Falls as a line segment of length k kilometers. Assume that your friends can hike d kilometers per day and that they are always correct when estimating whether they can reach the next stopping point during daytime. Let $s_1, s_2, \ldots, s_n$ denote the sorted set of distances from Baton Rouge to each of n stopping points.

Will this algorithm minimize the number of stops needed? If so, then explain why. If not, then explain why not.

Let $n = 2^h$ for some integer h. Consider a balanced ternary tree with n leaves; that is the tree is rooted, each non-leaf node has 3 children and all children are at the same level of the tree. A leaf ℓ has a bit $b_\ell \in \{0, 1\}$ associated with it.

For any node v of the tree, define its "value" α_v as follows:

$$\alpha_v = \begin{cases} b_v, & \text{if } v \text{ is a leaf} \\ \text{majority of the values of the children of } v, & \text{if } v \text{ is not a leaf} \end{cases}$$

Here the majority of three bits is the value that occurs at least twice.

The problem is to compute the value of the root of the tree.

(a) For $n = 9$, and input bits 0,0,0,1,1,1,0,1,0 (in order of leaves from left to right), draw the tree and label all nodes with their values.

(b) Prove that any algorithm to compute the value of the root must (in the worst case) read all n input bits.

(c) Consider the following recursive algorithm. If $n = 1$, the root is a leaf and its value is known. For $n > 1$, compute the values v_1, v_2 of the first two of the three children of the root. If $v_1 = v_2$, then the value of the root is $v_1 = v_2$. Otherwise, compute the value v_3 of the third child and this is the value of the root.

Determine the average time complexity of the algorithm assuming that (a) the input bits are distributed randomly (each input has equal probability of being a 0 or a 1), (b) reading an input requires unit time (c) all operations other than reading the input require no time. Justify your answer.

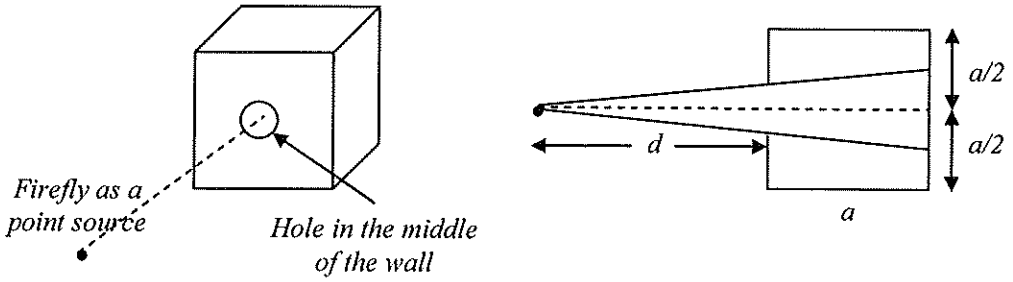
An undirected graph $G = (V, E)$ is said to be free of odd cycles, if there are no cycles of odd length. A cycle is said to be of odd length, if the number of vertices in the cycle is odd.

(a) Design the most efficient sequential algorithm possible to compute whether or not a graph is free of odd cycles. Analyze the running time of your algorithm. Argue why your solution is the most efficient.

(b) Consider an undirected graph $G = (V, E)$ that is free of odd cycles. Now suppose a new vertex u is added to the graph along with edges between u and a constant number of nodes $\in V$. In answering this part, you may assume some preprocessing of the graph along the lines of the algorithm in part (a). Design the most efficient sequential algorithm possible to compute whether or not a graph is free of odd cycles. Analyze the running time of your algorithm. Argue why your solution is the most efficient.

Computer Applications 1 Fall 2012

There is a firefly (acting as a point light source) outside a cube-shaped box. On one side of the box, there is small disk-shaped hole. (The radius of the hole is b.) The edge length of the cube is a. The distance between the firefly and the box is d. The radiance intensity of the firefly (point light source) is I. Light coming from the firefly forms a bright region inside the box.



(a) What is the solid angle subtended the light source and bright region?

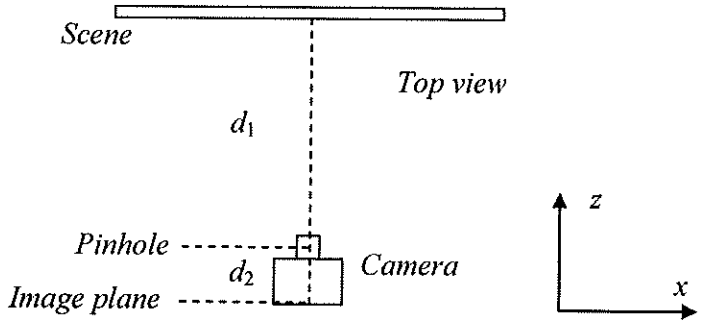
(b) What is the total power received by the bright region?

(c) What is the irradiance at the center of the bright region?

(d) The firefly starts to fly towards the box along the central axis, passes through the hole and hits the wall. Derive the formula for the irradiance as a function of the firefly position.

Computer Applications 2 Fall 2012

We take an image of a static planar scene. The camera, which is modeled as a pinhole camera, is at a fixed location as shown below; the distance between the scene and the pinhole of the camera is d_1. The distance between the pinhole and the image plane is d_2. The exposure time of the camera is t.



(a) The camera is moved during exposure along the x axis with a constant speed of V. The image appears blurry due to this movement. The blur can be formulated as follows:

$g(x,y) = h(x,y) * f(x,y)$

where g(x,y) is the blurry image, h(x,y) is the blur function, f(x,y) is the image that would be obtained if the camera was not moved, and "*" is the convolution operation.

(a1) What is h(x,y)?

(a2) We can take the Fourier transform of the above equation, and get G(u,v) = H(u,v)F(u,v). The blur-free image can be estimated as F'(u,v) = G(u,v)/H(u,v). However, the zero-crossings of H(u,v) pose a problem in the restoration. Where do the zero-crossings occur in the (u,v) plane?

(b) Suppose that the camera is moved during exposure along the z axis with a constant speed of V. What is the blur function?

(c) Suppose that the camera is rotated along the z axis with an angular velocity of W. What is the blur function?

Computer Applications – Question 4 **Fall 2012**

Let $P = \{p_1, p_2, \ldots, p_n\}$ be a set of unsorted points located on the x-axis and their coordinates are stored in an array. Now given two numbers a, b, indicating the interval $[a, b]$ on the x-axis, we want to output all the points inside this interval.

a. Suppose we only need to do a one-time query for $[a, b]$, what is the fastest way to do this? Analyze the time complexity in big-O notation.

b. Suppose need to do many different queries, i.e., to check for many intervals $[a_i, b_i], i = 1, 2, \ldots, m$, where $m > n$. Since P is fixed, we can preprocess P using a binary search tree (BST), then perform all queries using it. Elaborate your query algorithm and analyze its time complexity in big-O notation.

c. The BSTs of a given P are not unique. For a set P with n points, derive how many different BSTs you may construct? Suppose all the n points in P are distinct from each other.

Computer Application 5 **Fall 2012**

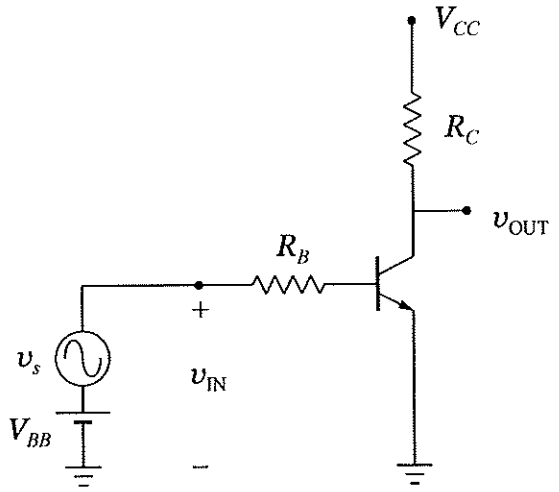
(a) Assume that you have been assigned the 200.35.1.0/24 network block. Define an extended-network-prefix that allows the creation of 20 hosts on each subnet. What is the maximum number of hosts that can be assigned to each subnet? What is the broadcast address for subnet 200.35.1.192/27?

(b) A group of $2^n - 1$ routers are interconnected in a centralized binary tree, with a router at each tree node. Router i communicates with router j by sending a message to the root of the tree. The root then sends the message back down to j. Derive an approximate expression for the mean number of hops per message for large n, assuming that all router pairs are equally likely.

(c) In most networks, the data link layer handles transmission errors by requesting damaged frame to be retransmitted. If the probability of a frame's being damaged is p, derive the mean number of transmissions (T) required to send a frame if acknowledgements (ACKs) are never lost? What will happen to T if ACKs can also be lost with probability p.

Circuits and Systems
Problem 1

Consider a bipolar junction transistor circuit shown below with $R_C = 2.2\ \text{k}\Omega$, $R_B = 22\ \text{k}\Omega$, $V_{BB} = 1.2$ V, and $V_{CC} = 12$ V. Assume $\beta = 100$, $V_f = 0.7$ V, and $V_{sat} = 0.2$ V for the transistor.



(a) Plot the transfer characteristic, v_{OUT} versus v_{IN}, of the circuit.

(b) When $v_s = V_p \cdot \sin(2\pi ft)$, find the largest value for V_p without the transistor going into saturation or cutoff regions. If needed, assume $f = 1$ kHz.

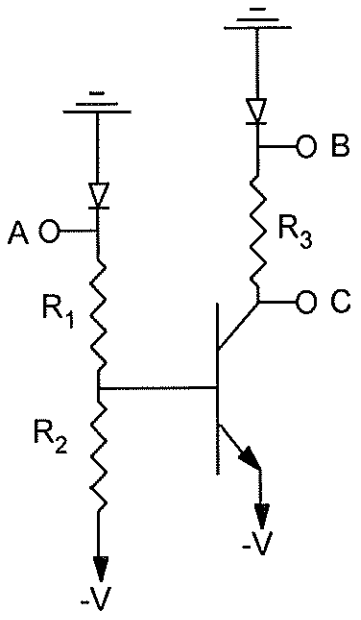
(c) Adjust R_C and R_B to double V_p while maintaining the other conditions in (b). Then, present your opinion in detail whether this circuit would be better than the original circuit or not.

Circuits and Systems
Problem 2

a) In the circuit below R_1 = 100 kΩ, R_2 is an open circuit, and R_3 = 1kΩ. Find the voltage at the collector, V_C, if β = 50 and -V is -10 Volts.

b) In the circuit below R_2 is again an open circuit, and R_3 = 0. No information is given about the other components. Find an expression for β in terms of V_A and V_B.

c) In the circuit below R_1 = R_2 = 100 kΩ, R_3 = 1kΩ, and β = 50. Find the value of the voltage, -V, which maximizes the difference between V_A and V_B.



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Circuits and Systems
Problem 3

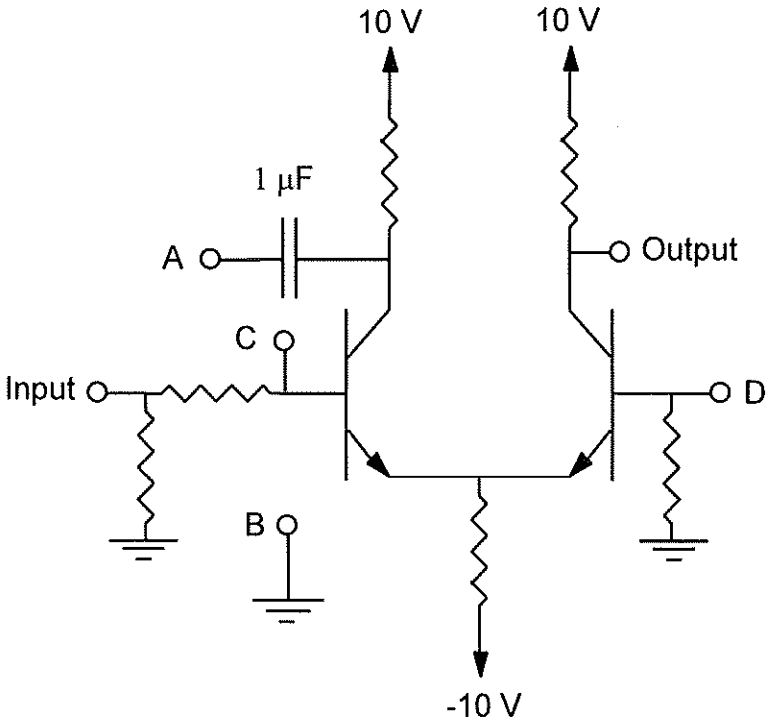
In the circuit below both transistors have very high current gain, β. All the resistors are 1000 Ohms.

a) The output is a 1 Volt p-p square wave with a risetime T. Estimate the amplitude and rise time of the input.

b) Point A is connected to point B. Estimate the rise time of the output.

c) Point A is connected to point C. Estimate the rise time of the output.

d) Point A is connected to point D, making the circuit oscillate with no input. Estimate the frequency at which it oscillates.



Circuits & Systems
Problem #4

The circuit shown in the following is a CMOS differential stage in which the aspect ratio W/L is indicated adjacent to devices. The NMOS devices have k = 25 $\mu A/V^2$, V_T = 1.5 V, and V_A (BJT equivalent Early voltage) = $1/\lambda$ = 100 V; the PMOS devices have k = 12.5 $\mu A/V^2$, V_T = -1.5 V, and $V_A = 1/\lambda$ = 50 V.

Given:

$V_{GS8} = V_{DS8}$ = 3.45 V

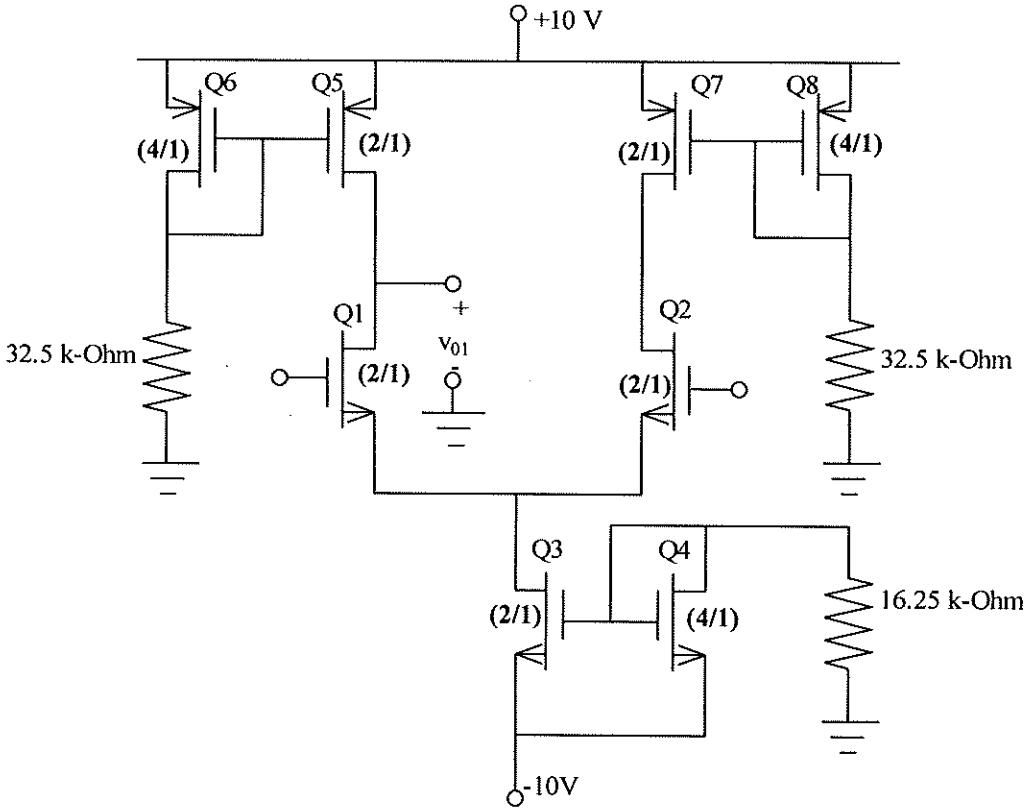
$I_D = [\{0.5\mu C_{OX}\}(W/L)(V_{GS}-V_{th})^2(1+\lambda V_{DS})]$

Where λ is the channel length modulation parameter and $k = 0.5\mu C_{OX}$. I_D is the drain current, μ is the mobility of the carrier in the channel region, V_{th} is the threshold voltage. C_{ox} is the gate-oxide capacitance per unit area.

(a) Determine the bias currents in Q3, Q5, and Q7.

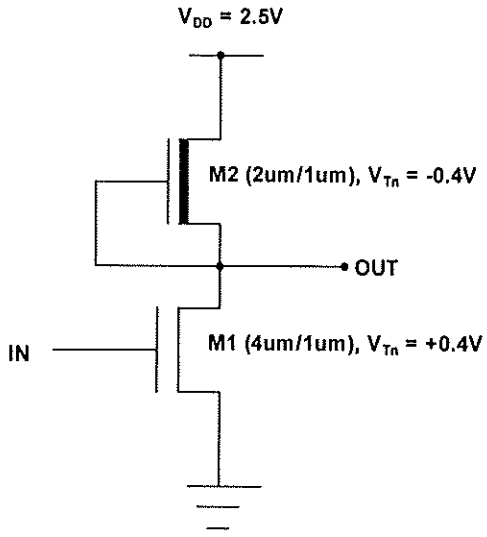
(b) Evaluate $|A_{DM}|$ and the CMRR.

(c) What will happen to CMRR if $1/\lambda$ of n-MOS current source is increased to 200V?



Circuits & Systems
Problem #5

Consider the following circuit. Device M1 is a standard NMOS device. Device M2 has all the same properties as M1, except that its device threshold voltage is *negative* and has a value of –0.4V. Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device M2 are the same as a regular NMOS. Assume that the input *IN* has a 0V to 2.5V swing. Note: Use SPICE MOS Model LEVEL 1 equations.



a) Device M2 has its gate terminal connected to its source terminal. If V_{IN} = 0V, what is the output voltage? In steady state, what is the mode of operation of device M2 for this input?

b) Compute the output voltage for V_{IN} = 2.5V. You assume that V_{OUT} is small to simplify your calculation. In steady state, what is the mode of operation of device M2 for this input?

c) Assuming switching activity, $Pr_{(IN=0)}$ = 0.3, what is the static power dissipation of this circuit? Use V_{DS} = 0.63V in calculation.

Given: SPICE MOS Model Level 1 Equations:

$I_D = 0.5\mu C_{OX}(W/L)\{2(V_{GS}-V_{th})V_{DS}-V_{DS}^2\}$ (Linear region)
$I_D = 0.5\mu C_{OX}(W/L)\{(V_{GS}-V_{th})^2\}$ (Saturation region)
Where V_{GS} is the gate-to-source voltage and I_D is the drain current and
μC_{OX} = KN (process transconductance parameter)

$KN_{M2}/KN_{M1} = 1$; $KN_{M2} = 115\mu A/V^2$

Physical Electronics
Problem 1

An abrupt silicon p-n junction has acceptor atom density $N_A = 10^{18}$ cm^{-3} on one side and donor atom density $N_D = 5 \times 10^{15}$ cm^{-3} on the other side.

a) For this diode, calculate the Fermi level positions in the n-region and the p-region. (20%)
b) Draw an equilibrium energy band diagram for this diode based on your results in a) above. Label the diagram carefully indicating all pertinent values. (25%)
c) What is the built-in equilibrium junction potential V_{bi} from the diagram in b)? (15%)
d) Contact potential in a diode is frequently given by: $V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$. Compare the value obtained by this equation to the value obtained in c) above. Comment on discrepancy, if any. (20%)
e) If now the value of N_A is increased to 5×10^{19} cm^{-3} without changing the value for N_D, how will you determine the value for V_{bi}? Would you use the approach in step c) or in step d) above or neither? Explain clearly. Comment on the validity of your answer explaining assumptions made, if any. (20%)

Temperature T = 300 K, Boltzmann constant $k = 1.38 \times 10^{-23}$ J/K, band gap of Si = 1.1 eV, effective density of states in Si at 300 K in conduction and valence bands, N_C and N_V, are respectively 2.8×10^{19} cm^{-3} and 1.04×10^{19} cm^{-3}, magnitude of electron charge $q = 1.6 \times 10^{-19}$ C, intrinsic carrier density n_i in Si at 300 K = 1.5×10^{10} cm^{-3}.

Physical Electronics
Problem 2

Incident light with *uniform* generation rate of 10^{16} $cm^{-3}s^{-1}$ creates electron-hole pairs in a uniformly doped semiconductor film of thickness t = 50 μm and cross-section area of 0.5 cm^2. The life time of excess carriers in this material is 10^{-6} s. The electron and hole mobility values in this material are respectively 1000 and 150 cm^2/V.s. The film is connected to a 10 V battery as shown in the figure below.

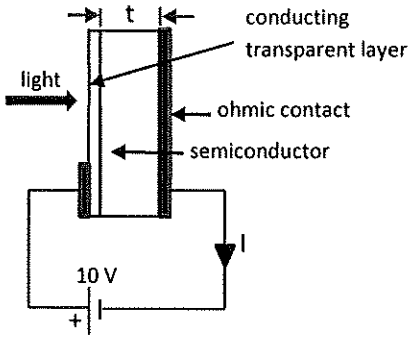
a) Determine the average excess carrier concentration of electrons and holes in this semiconductor film in steady state. Give reasons for your answer. (25%)

b) Determine the change in current $\Delta I = I_{light} - I_{dark}$, where I_{light} is value of current I with light and I_{dark} is value of I without incident light. Show intermediary details. (35%)

c) How will the value of ΔI change if thickness t is increased, all other things remaining same? *Explain* clearly. A qualitative answer is needed. (20%)

d) How will the value of ΔI change if battery voltage is increased to higher values compared to case b) above? *Explain* clearly. A qualitative answer is needed. (20%)

Magnitude of an electron charge q = 1.6×10^{-19} C. Carrier saturation velocity in the semiconductor = 2×10^6 cm/s.

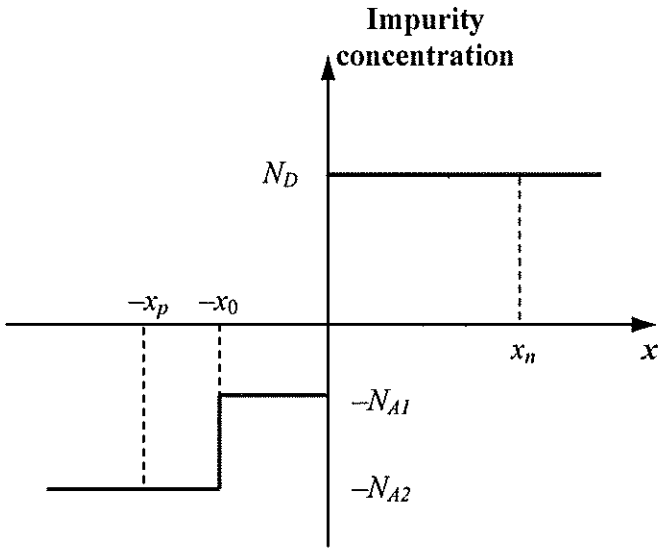


Physical Electronics
Problem 3

A *p-n* junction diode has the doping profile as shown in the figure below. N_D and N_A are donor concentration and acceptor concentration, respectively. Given,

$$p_0 = n_i \exp\left(\frac{E_i - E_F}{kT}\right) \quad \text{and} \quad n_0 = n_i \exp\left(\frac{E_F - E_i}{kT}\right)$$

where n_i is the intrinsic carrier concentration, E_i is the intrinsic Fermi level, E_F is the Fermi level, k is the Boltzmann constant and T is the temperature. n_0 and p_0 are electron and hole concentrations in equilibrium. x_n and x_p are *n*-side and *p*-side widths of the *p-n* junction depletion region. Assume that $-x_p < -x_0$ for all applied biases of interest.



Given, $N_D = 5 \times 10^{15}$ cm^{-3}, $N_{A1} = 1 \times 10^{16}$ cm^{-3}, $N_{A2} = 2 \times 10^{16}$ cm^{-3}, and $x_0 = 1$ μm.

(a) Assuming impurities are 100% ionized, derive the expression for the built-in potential at thermal equilibrium. Justify your answer and show detailed steps.

(b) Calculate the built-in voltage (V_{bi}), x_n, and x_p.

(c) Draw an equilibrium band diagram.

(d) When a forward bias of 0.3 V is applied, repeat (b).

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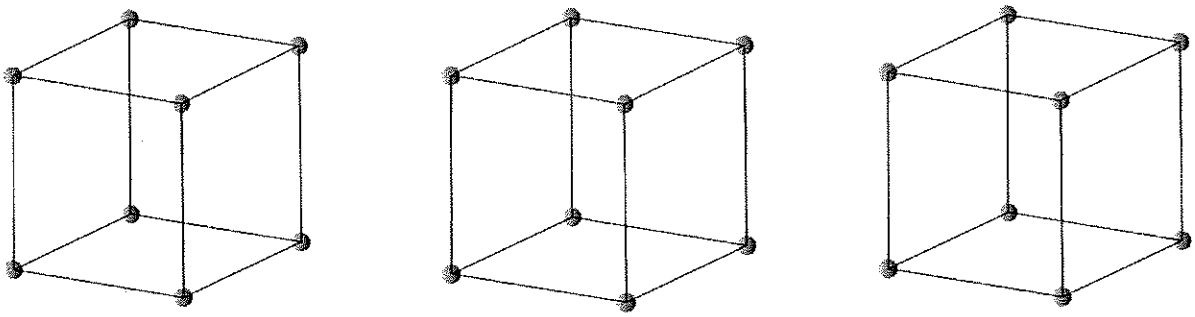
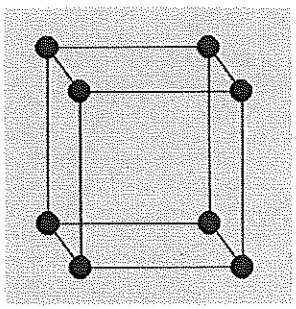
Physical Electronics
Problem 4

[1] Consider the following cubic crystal structures and answer the questions below. Clearly indicate your final answer for each problem.

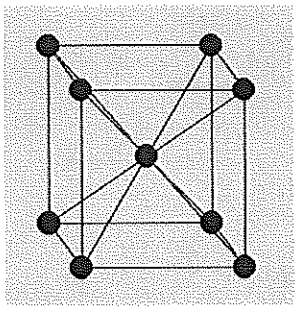
a) Three identical simple cubic (sc) structures are shown. Draw the (111), (100), and (110) planes. Use one cube for each plane.



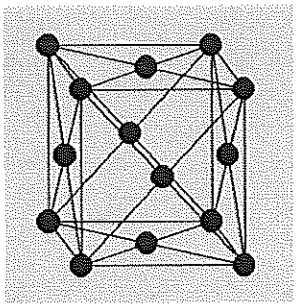
b) Calculate the volume (V) of the conventional unit cell for a simple cubic (sc), a body-centered cubic (bcc), and a face-centered cubic (fcc) crystal lattice. Assume a lattice constant of a = 4 Å for each structure. Show units in final answer.



sc



bcc



fcc

V_{sc} = _____ V_{bcc} = _____ V_{fcc} = _____

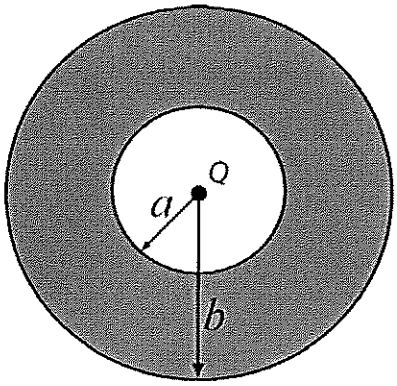
c) Calculate the volume (V_p) of the primitive unit cell for a simple cubic (sc), a body-centered cubic (bcc), and a face-centered cubic (fcc) crystal lattice. Assume a lattice constant of a = 4 Å for each structure. Show units in final answer.

$V_{p(sc)}$ = _____ $V_{p(bcc)}$ = _____ $V_{p(fcc)}$ = _____

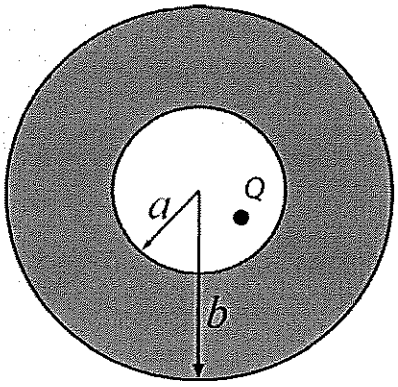
Physical Electronics
Problem 5

Consider a point charge Q at the center of a spherical metallic shell of inner radius a and outer radius b (Figure (a)).

(a) Find the induced surface charge density on the inner and outer surface of the metallic shell.
(b) Find and plot the electric field as a function of the radial distance r.
(c) Find the electrostatic potential difference between the points $r=0.5a$ and $r=2b$.
(d) Find the electrostatic potential difference between the points $r=a$ and $r=b$.
(e) If the point charge Q is moved to a point off from the center of the shell (Figure (b)), find the electric field for $r>b$.



(a)



(b)

Develop current and power equations for single-phase, harmonic generating loads. Apply these equations to a resistor switched ON/OFF by a TRIAC. Assume that the TRIAC is connected as shown on Fig. 1 and the load is supplied with sinusoidal voltage

$$u = \sqrt{2}\,U \sin\omega_1 t$$

such that $U = 220\text{V}$, $R = 1\ \Omega$, and TRIAC firing angle $\alpha = 135^0 = ¾\ \pi$.

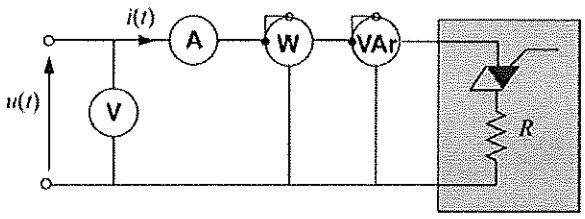


Figure 1.

Figure 2 shows the structure of PWM inverter applied as a switching compensator.

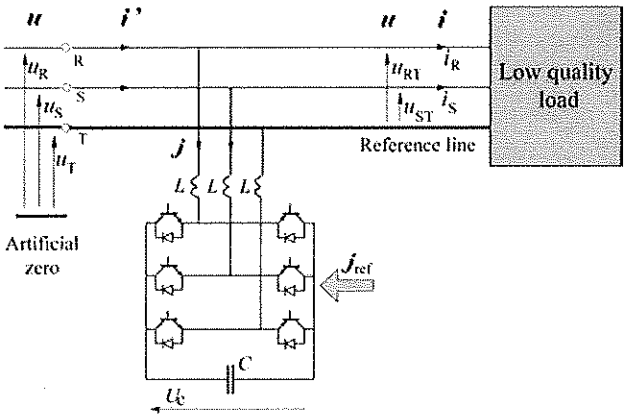


Figure. 2

Explain fundamentals of the vector control of such a compensator.

1) Draw the circuit diagram of a DC separately excited motor and write the instantaneous voltage equations for both: armature and field winding (including inductances). Write the torque equation including friction, load torque and inertia.

2) Draw the block diagram of a DC motor loaded by the load torque $T_L = C\omega_m$ (C-constant, ω_m-rotor speed), which allows to calculate the speed ω_m at a given supply voltage V.

3) Draw the block diagram of PI controller connected to the plant of $G_p(s)$ transfer function with the unity feedback loop and write its transfer function.

4) Draw the block diagram of DC separately excited motor with the current and speed PI control loops. What is the value of speed error in steady state operation?

1) The circuit diagram of a ferromagnetic bar suspended by the magnetic field is shown in Fig. 1.

   Write down the voltage equation and motion equation of the system defined by the following parameters:
   - Coil resistance R_1
   - Coil inductance L_1
   - Friction coefficient D,
   - Mass of the suspended bar M.

   Write the expression for the magnetic force f_m in terms of the current i_1.

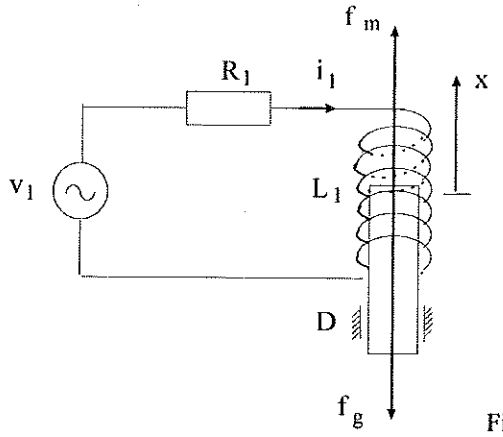


Fig. 1

2) Fig. 2 shows the motor with round stator and salient pole rotor.

   Write the voltage equations for two windings and equation for electromagnetic torque acting on the rotor. The rotor winding of inductance L_2 and resistance R_2 is supplied by the voltage v_2 and a stator winding of inductance L_1 and resistance R_1 is supplied by the voltage v_1. Name the torque components acting on the rotor.

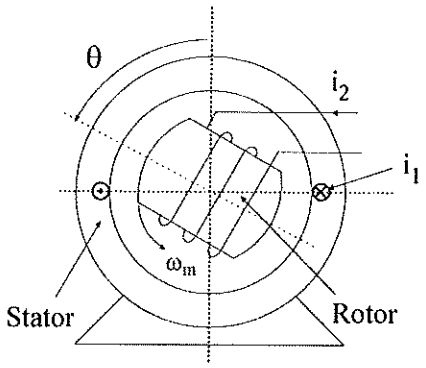


Fig. 2

3) Fig. 3 shows the scheme of *jumping ring*. The coil of inductance L_1 and resistance R_1 is connected to the voltage source of voltage v through the capacitor of capacitance C. The aluminum ring has the resistance R_2 and inductance L_2.

   Draw the circuit diagram of the system and write the voltage equations for coil and ring knowing that their self inductances do not change but the mutual inductance M changes with the distance x between them

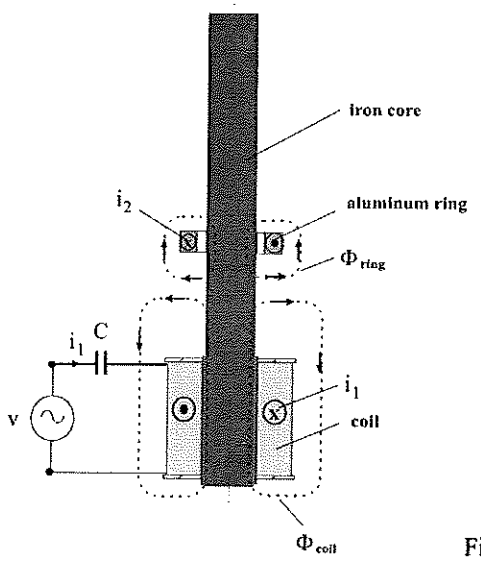


Fig. 3

4) Fig. 4 presents the single phase motor with the stator winding of resistance R_1 and inductance L_1 supplied with the voltage v_1. The rotor winding of resistance R_2 and inductance L_1 is supplied with the voltage v_2. The mutual inductance between two windings is M. All inductances are the function of angle θ.

Write the voltage equations for two windings and the expression for torque acting on the rotor. What are the torque components acting on the rotor?

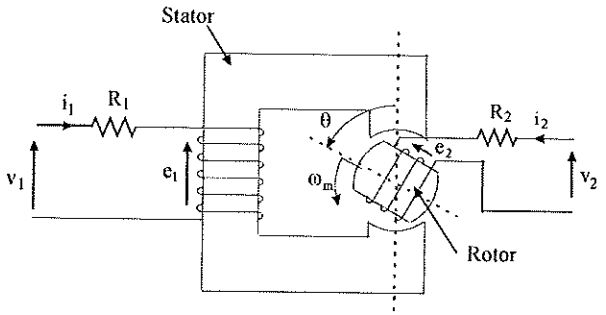
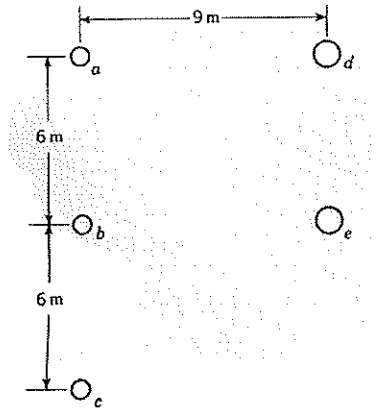


Fig. 4

One circuit of a single-phase transmission line is composed of three solid 0.25-cm-radius wires. The return circuit is composed of two 0.5-cm-radious wires. The arrangement of conductors is shown in the following figure. Find the inductance due to the current in each side of the line and the inductance of the complete line in Henrys per meter (and in milihenrys per mile.)



AUTOMATIC CONTROL 1 **FALL 2012**

Let $G_1(s)$ and $G_2(s)$ have the following state space realizations

$$G_1(s) = C_1(sI - A_1)^{-1}B_1 + D_1, \;\; G_2 = C_2(sI - A_2)^{-1}B_2 + D_2$$

1. Find a state space realization for $G(s) = G_1(s)G_2(s)$.
2. Now let $G_1(s) = \dfrac{5(s+2)}{s(s+1)}$ and $G_2(s) = \dfrac{2}{s+2}$. Use the realizaiton in (1) to find a state space realization of $G = G_1G_2$. Is this realization controllable? Is this realization observable?
3. Is the realization in (2) stabilizable? Is it detectable? Can you find a state feedback so that the closed-loop poles are at $-5, -5, -5$?

AUTOMATIC CONTROL 2 **FALL 2012**

Let a transfer matrix be give by

$$G(s) = \begin{bmatrix} \frac{1}{s(s+1)} & \frac{1}{s+1} \\ \frac{10}{s} & \frac{90}{(s+2)^2} \end{bmatrix}$$

1. Find a minimal (controllable and observable) realization for G.
2. Find the transmission zeros of the system.
3. Suppose that $z > 0$ is the transmission zero computed from above, find a v such that $G(z)v = 0$. Next find the time response of the system when $u = ve^{zt}$.

AUTOMATIC CONTROL 3 **FALL 2012**

Suppose a single input control system

$$\dot{x} = Ax + bu$$

is controllable.

1. Under what condition $\dot{z} = Az + Abv$ is also controllable?
2. Suppose $u = Kx$ is a desired state feedback for the system $\dot{x} = Ax + bu$. Find a state feedback $v = Fz$ for $\dot{z} = Az + Abv$ so that $A + bK$ and $A + AbF$ have the same eigenvalues.

AUTOMATIC CONTROL 4 **FALL 2012**

Consider the unity negative feedback system with open loop transfer function given by

$$KG(s) = \frac{K}{s(s-1)(s+6)}.$$

(i) Sketch its root locus for $K \geq 0$.

(ii) Suppose that a lead compensator is added in and thus the open loop transfer function is given by

$$KL(s) = \frac{K(s+1)}{s(s-1)(s+6)(s+20)}.$$

Find the range of $K \geq 0$ such that the closed-loop system is stable.

(iii) Sketch root locus for $KL(s)$ with $K \geq 0$: you need to estimate the number and the location of the break points without computing the roots of $a'(s)b(s) - b'(s)a(s) = 0$; and you need to estimate the $j\omega$ crossing points without computing their exact values.

AUTOMATIC CONTROL 5 **FALL 2012**

Consider the unity negative feedback system with open loop transfer function given by

$$KG(s) = \frac{K(s+1)}{s(s-1)}.$$

(i) Sketch its Nyquist plot and find the stability range of K.

(ii) Find $K > 0$ such that the closed-loop system has damping ratio $\zeta = \sqrt{2}/2$. What is the corresponding natural frequency ω_n?

(iii) Design a lead compensator such that the closed-loop system has the same damping ratio $\zeta = \sqrt{2}/2$ as in (ii), and the natural frequency $\omega_n \geq 10$.

(iv) For the design in (iii), estimate the percentage overshot for the closed-loop system.

Consider a set of finite duration waveforms $\mathcal{S} = \{s_1(t), \cdots, s_M(t), 0 \leq t \leq T\}$, where T is the symbol duration, whose prior probability distribution is given by $\{P_i, 1 \leq i \leq M\}$, and $1 \geq P_i \geq 0$ is the probability of sending the i-th waveform $s_i(t)$ satisfying $\sum_{i=1}^{M} P_i = 1$. Assume one of M waveforms is picked each time under the above prior probability distribution and then transmitted over an additive white Gaussian noise channel with power spectral density $S_N(f) = N_0/2$ for all f, where N_0 is a positive constant. Answer the following questions:

1. Compute P_S, the average transmission power of the given waveform set $\mathcal{S}$.
2. Let $r(t) = s(t) + n(t)$ for $t \in [0, T]$ and $s(t) \in \mathcal{S}$ denote the received signal. Provide a block diagram to illustrate how to process $r(t)$ so that the average symbol error probability can be minimized, and show that the statistics obtained from your block diagram are sufficient to make such a decision.
3. If it is possible to transform the set $\mathcal{S}$ to another set of M waveforms under the same prior probability distribution and the same average symbol error probability but with a reduced average power expenditure, how to achieve that goal?
4. If the additive noise $n(t)$ in the received signal $r(t) = s(t) + n(t)$ is a white, but non-Gaussian wide-sense stationary random process, will the receiver designed for the Gaussian case still be optimal in terms of minimizing the average symbol error probability and why?

The output $y(t)$ of a linear time invariant system is related with its input $x(t)$ by the following differential equation:

$$\frac{dy(t)}{dt} + 10y(t) = x(t)$$

1. Determine the impulse response $h(t)$ and its continuous time Fourier transform (FT) $H(j\omega)$ of this system, where $j = \sqrt{-1}$.
2. For an input $x(t) = u(t)$, find its output $y(t)$ and its Fourier transform $Y(j\omega)$.
3. If $x(t)$ is a zero mean Gaussian random process whose power spectral density is $S_x(f) = N_0/2$ for all $f = \frac{\omega}{2\pi}$, compute the auto-correlation function of the output random process $y(t)$, and show if it is possible to get a sequence of identically and independently distributed random variables $\{y(iT)\}$ by sampling $y(t)$ at $t = iT$, for some constant $T > 0$.

A linear-time-invariant system is characterized by its discrete-time Fourier transform (DTFT), which is

$$H\left(e^{j\omega}\right) = \frac{\prod_{i=1}^{2}\left(e^{j\omega} - \alpha_i\right)\left(e^{j\omega} - \alpha_i^*\right)}{e^{j4\omega}},$$

where $j = \sqrt{-1}$, α_i^* is the complex conjugate of α_i, the real parts of α_i's are not zero, and $0 < |\alpha_1| < 1 < |\alpha_2|$. An *equalizer* $G\left(e^{j\omega}\right)$ is the reciprocal of $H\left(e^{j\omega}\right)$ such that $G\left(e^{j\omega}\right) H\left(e^{j\omega}\right) = 1$.

1. Determine the transfer functions (z-transforms) $H(z)$ and $G(z)$ corresponding to $H\left(e^{j\omega}\right)$ and $G\left(e^{j\omega}\right)$, respectively.
2. Determine the region of convergence (ROC) for $H(z)$.
3. Determine the region of convergence (ROC) for $G(z)$.
4. The inverse z-transform of $G(z)$ is denoted by $g[n]$, $-\infty < n < \infty$. Assume that $g_M[n]$ is the truncated version of $g[n]$ such that

$$g_M[n] = \begin{cases} g[n], & -M \leq n \leq M \\ 0, & \text{otherwise} \end{cases}$$

where M is an arbitrary positive integer. Denote the *approximation error* ξ_M by $\xi_M = \sum_{n=-\infty}^{\infty} \left|g[n] - g_M[n]\right|^2$. Prove that ξ_M is strictly monotonically decreasing with respect to M, i.e., $\xi_M > \xi_{M+1}, \forall M \geq 1$.

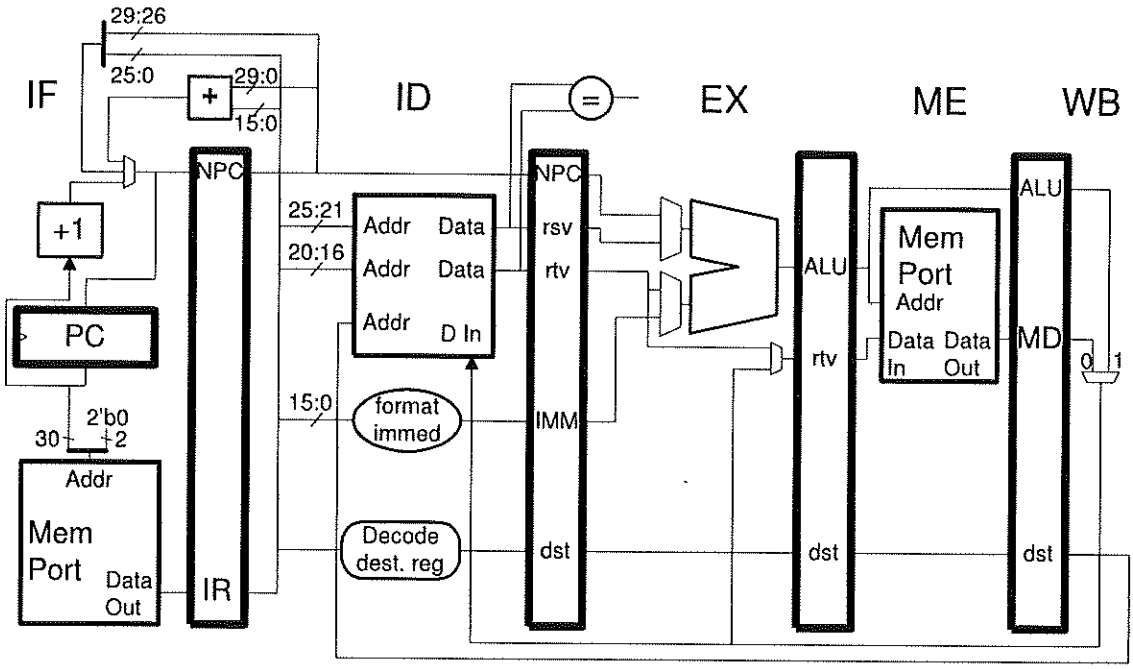
White noise with power spectral density $S_X(f) = N_0/2$ is applied to a filter with impulse response $h(t) = 1$ for $0 < t < 1$ and 0 otherwise.

1. Find the cross power spectral density $S_{XY}(f)$.
2. Find the cross-correlation $R_{XY}(\tau)$.
3. Find the output power spectral density $S_Y(f)$.
4. Find the output auto-correlation $R_Y(\tau)$.
5. Find the output power P_Y.

$\{X_n\}$ is a random process with mean function $E[X_n] = \mu(n)$ and autocorrelation function $E[X_n X_m] = R(n, m)$.

1. What is meant by the statement that $\{X_n\}$ is wide sense stationary (WSS)?
2. What is meant by the statement that $\{X_n\}$ is strictly stationary?
3. Suppose $\{X_n\}$ is an independent and identically distributed random porcess. Carefully state the Weak Law of Large Numbers (WLLN) for $\{X_n\}$. You must give the conditions for which the WLLN holds.
4. Suppose $\{X_n\}$ is a WSS Gaussian random process. Prove that it is a strictly stationary process.

Illustrated below is a MIPS implementation in which the branch is resolved in ID, but which **lacks** bypass paths into the EX stage. The register file, in ID, is designed so that a read of a register that is also being written will return the value being written.



(*a*) Show a pipeline execution diagram for the MIPS code below assuming that the branch is taken. Pay close attention to bypass paths (or their absence) and be sure that the number of stall cycles in your solution is correct.

```
 beq r20, r21, TARG
 add r1, r2, r3
 andi r14, r14, 0xff
 and r12, r1, r13
TARG:
 sub r4, r1, r5
```

(*b*) Show a pipeline execution diagram for the MIPS code above assuming that the branch is not taken.

For the parts below consider a variant of MIPS called *MIPS Exposed!! (MIPSe!!)*, in which the behavior of an instruction is defined to be whatever the illustrated pipeline would do if it didn't stall.

(*c*) The code below is identical to the code above, but it is written for MIPSe!!. Re-write the code for MIPS.

```
 beq r20, r21, TARG
 add r1, r2, r3
 andi r14, r14, 0xff
 and r12, r1, r13
TARG:
 sub r4, r1, r5
```

Call the outcome of a branch either taken (T) or not taken (N), the *local history* of a branch is a sequence of its outcomes. For example, a branch with local history TTN has three outcomes, the most recent not taken.

A *local history predictor* predicts a branch by using its local history as an index (an address) into a *pattern history table (PHT)* in which 2-bit counter values are stored. The branch is predicted not taken if the count is 0 or 1, otherwise it is predicted taken. If the branch is ultimately taken the counter is incremented otherwise it is decremented. Let m denote the number of bits in the PHT index (address).

Call pattern TTNTTNTTN... a 3-iteration loop pattern, generated by a 3-iteration loop branch; define an i-iteration loop pattern and branch similarly.

(*a*) Consider the local history predictor described above in which m bits of a branch's local history is used to index the PHT. **Ignoring interference** from other branches, what is the longest i-iteration loop branch (largest i) that can be predicted with 100% accuracy on this predictor. Use an example to justify your answer.

(*b*) Explain why the answer to the question above would be different if one did not ignore interference from other branches. Consider common branch behaviors, and illustrate your answer with an example.

For the next parts consider two methods to reduce interference between branches: *LH xor PC indexing* and *LH cat PC indexing*. In LH xor PC indexing the m-bit PHT index is the m-bit local history exclusive ored with m bits of the PC (address) of the branch being predicted. In LH cat PC indexing the m-bit PHT index is the $\frac{m}{2}$-bit local history concatenated with $\frac{m}{2}$ bits of the branch PC.

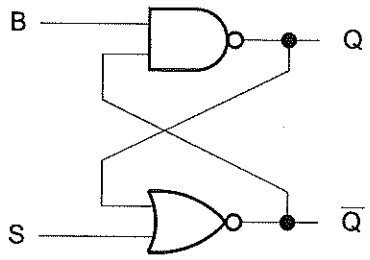
(*c*) Which of the two methods would be better for the loop branches described above? Explain.

(*d*) Suppose a program had a frequently executing branch that could be modeled as a Bernoulli random variable, with probability of being taken switching from $p = .2$ to $p = .8$ every million executions of the branch. Which of the two methods would be better for this random branch? Explain, and also explain the impact on short perfect loop branches.

Computer Hardware 5 **Spring 2011**

This problem involves the utility of some fictitious hardware elements defined below. Answer the following questions. All answers must be justified.

(a) Consider the BS-latch represented by the circuit to the right.
Trace the response of the BS latch for the four possible logic values of the inputs.

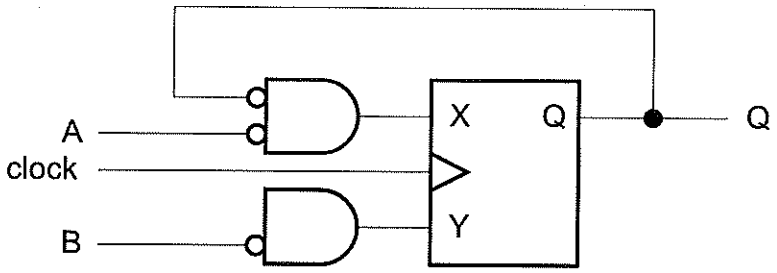


(b) Is the BS latch useful for designing sequential logic? Justify your answer.

(c) The function table to the right describes a fictitious XY flip-flop. Variables Q and Q^* refer to the present and next state, respectively, of the flip-flop.

X	Y	Q^*
0	0	1
0	1	Q
1	0	$\overline{Q}$
1	1	1

Determine the state diagram of the circuit shown below, that employs the XY flip-flop.



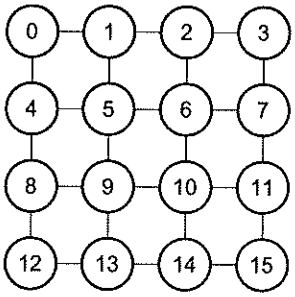
(d) Prove that every sequential circuit can be constructed using only XY flop-flops and combinational logic.

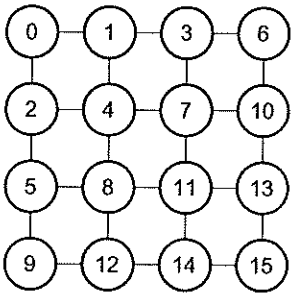
Consider an undirected graph $G = (V, E)$. We define an edge of G to be a *cycle-enabling* edge if its removal renders the graph acyclic. Design an efficient sequential algorithm to determine the set of all *cycle-enabling* edges of an undirected graph. Provide an analysis of its running time. Explain why your algorithm is correct. You will get no points if the complexity of your algorithm equals or exceeds $O(|V||E|)$.

Computer Software 2 **Spring 2011**

An $N \times N$ mesh topology is an N-row n-column arrangement of nodes with edges between a node and its neighbors to the north, south east and west. For $0 \leq i, j < N$, the node at row i and column j has a two-dimensional index (i, j). The *neighbors* of node (i, j) are nodes $(i-1, j)$, $(i+1, j)$, $(i, j-1)$ and $(i, j+1)$ (if they exist).

There are several possible one-dimensional numberings for an $N \times N$ mesh. The figures below shows two; *row-major* on the left and *diagonal* on the right.





For any node (i, j) of an $N \times N$ mesh, let $f(i, j)$ be a 1-dimensional number of the node. For any neighbor (i', j') of (i, i), the *distance* between (i, j) and (i', j') is defined to be $|f(i, j) - f(i', j')|$, the absolute value of the difference of their indices. The *average distance* of node (i, j) is the average of its distances from all its neighbors.

Some geometric problems benefit from a 1-dimensional numbering that tends to keep the numbering of neighboring nodes close to each other. That is, they prefer 1-dimensional numberings for which nodes have a small average distance.

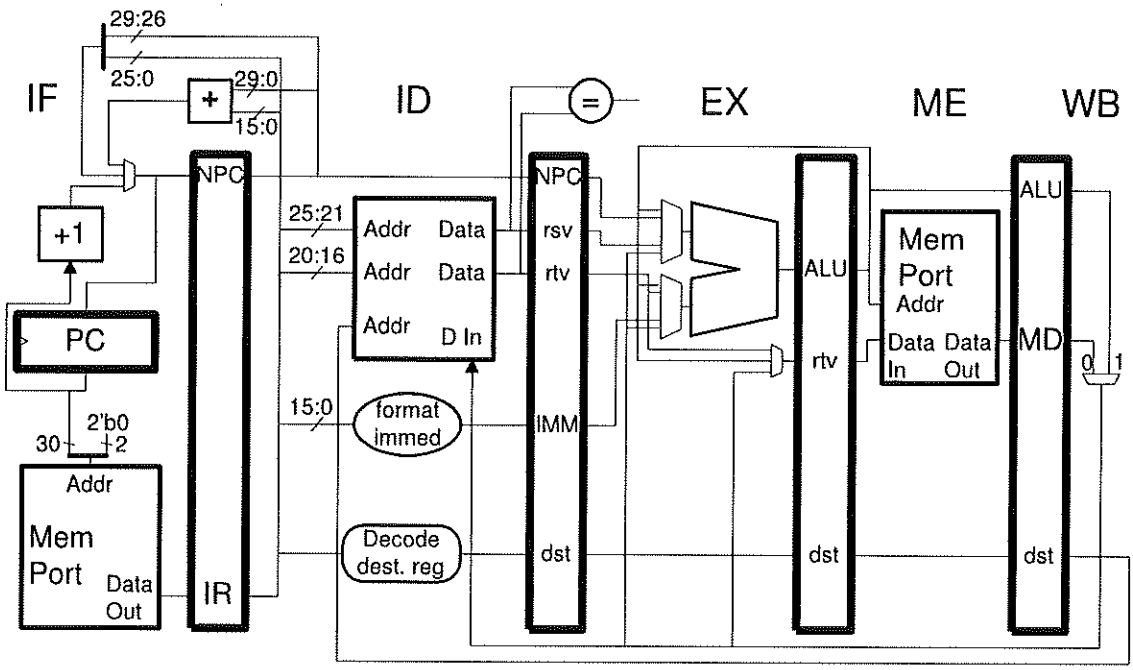
Answer the following questions. All answers must be justified.

(a) For a 4×4 R-Mesh, determine the average distance of node $(2, 2)$ under the two numberings (row major and diagonal) shown above.

(b) For any $N \geq 1$, and any $0 \leq i, j < N$, determine the average distance of node (i, j) of an $N \times N$ Mesh under the row major and diagonal numberings.

(c) Can you think of a way of numbering nodes that could have a smaller average distance for most nodes than in row major or diagonal numbering?

The MIPS code below executes on the illustrated implementation. It includes a prefetch instruction that will bring data to the cache for later use (to avoid a cache miss or at least reduce cache miss time seen by the load).




```
LOOP:
 lw r1, 0(r2)          # Load data at address 0+r2 into register r1.
 add r3, r3, r1
 add r2, r2, 4
 bneq r2, r4 LOOP      # Branch if r2 is not equal to r4
 prefetch 0x400(r2)    # Delay slot, executed whether or not branch taken. This
                       # instruction loads data at address 0x400+r2 into the cache.
```

A loop is said to be *unrolled by degree d* if the loop body is duplicated d times; if the loop executed I iterations before unrolling it would execute $\lfloor \frac{I}{d} \rfloor$ iterations after unrolling, for convenience assume that I is a multiple of d. Degree 1 indicates no unrolling at all.

(*a*) Show the code when the loop is unrolled by degree 2. Take care to apply appropriate optimizations. A goal is to reduce the instruction count and the number of stalls.

(*b*) Compare the performance of the unrolled and original loop. Use an appropriate performance measure. Assume that the load never misses the cache.

(*c*) Consider a processor similar to the one above except that load instructions never stall in `ME` due to a cache miss, instead they proceed through `WB` normally. If a load does miss then an instruction that tries to use the loaded value before it arrives will stall until the data arrives.

Suppose that the prefetch in the original code eliminates cache misses for the `lw`. To what degree would the code need to be unrolled to make the prefetch instruction unnecessary with no-stall loads? (Assume an unlimited number of registers.)

One approach to combat cheating in multiplayer computer games is to select multiple "referees" to monitor game play. Define the *average player-to-referees delay* for a player p_i as the average of the delays from p_i to each referee. Two criteria exist for selecting this set of referees:

1. minimize the sum over all players of the average player-to-referees delay, and
2. minimize the difference between the maximum average player-to-referees delay and the minimum average player-to-referees delay, where the maximum and minimum are taken over all players.

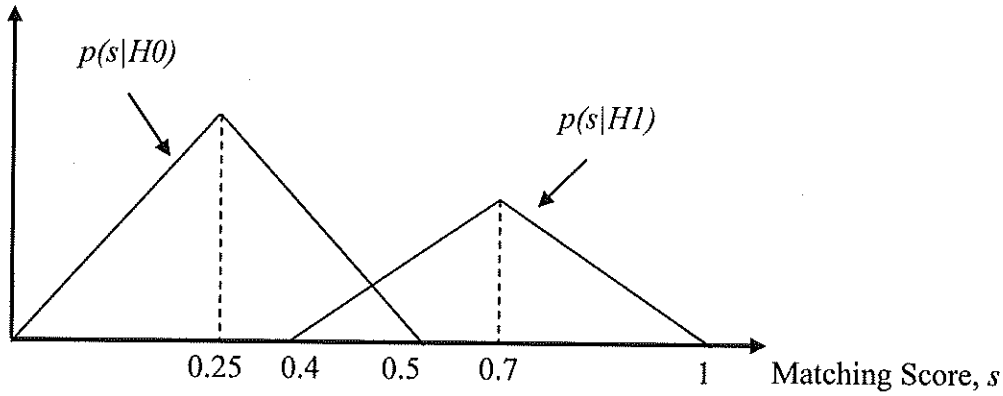
Design an algorithm to select r referees from a pool of z potential referees for a set of n players. You are given a table of the delays from each player to each potential referee. Your algorithm should be efficient and should try to satisfy both criteria as much as possible (but it might not be optimal for either criterion). What is the time complexity of your algorithm? Does it favor Criterion 1 over Criterion 2 or vice versa or does it address both equally?

Design a data structure to be used with a task scheduler as follows. Each task has a key, which is an arbitrary integer.

- When a new task arrives, insert the task into the data structure.
- When the task scheduler requests a task, then return the task with smallest key value and remove that task from the structure.

The structure is to execute these operations as efficiently as possible.

Describe in detail your data structure, the INSERT procedure, and the REMOVE-MINIMUM procedure. If the structure contains n tasks, then how much memory does it use? What is the time complexity of the INSERT procedure as a function of n? What is the time complexity of the REMOVE-MINIMUM procedure as a function of n?



A fingerprint verification system produces matching scores with distributions (probability density functions) as shown in the figure above, where

H0 is when the person is an imposter, that is, he is not who he claims he is;

H1 is when the person is genuine, that is, he is who claims he is.

The system verifies an identity if the matching score, s, is larger than a threshold T.

There is a risk (a scalar weight) associated with each misclassification. The risk of classifying an imposter as genuine is R0; and the risk of classifying a genuine person as an imposter is R1.

(a) Formulate the total risk as a weighted probability of error.

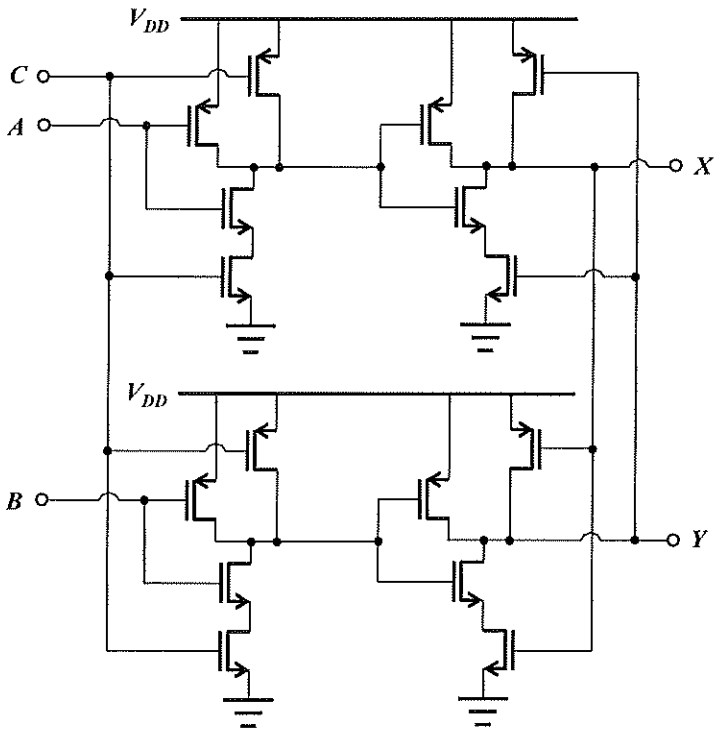
(b) Determine the optimal threshold value (that minimizes the total risk) when R0=R1.

(c) Determine the optimal threshold value when the risk of verifying an imposter is double the risk of declining a genuine person.

Spr 2011

Circuits and Systems
Problem 2

For a CMOS digital circuit given below, answer the following questions.



(*a*) Draw the gate-level diagram.

(*b*) Complete the truth table given below.

(*c*) Explain the function of the circuit.

Inputs			Outputs	
A	*B*	*C*	*X*	*Y*
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

AUTOMATIC CONTROL 1 **SPRING 2011**

Let a dynamical system be described by the following set of differential equations:

$$\ddot{x}_1 + 3\dot{x}_1 + 2x_1 = 2\dot{u} + 8u$$

$$\dot{x}_2 + ax_2 = x_1$$

$$y = x_1 + x_2$$

1. Find a state space realization of the system;
2. Discuss the controllability and observability of the system with respect to the parameter a.

AUTOMATIC CONTROL 2 **SPRING 2011**

Let a second order dynamical system be described by

$$\dot{x} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 2 & 1 \\ 0 & 0 & -4 \end{bmatrix} x + \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} u$$

$$y = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} x$$

1. Determine if the system is controllable, stabilizable, observable and detectable.
2. If possible, find a state feedback control so that the closed-loop poles are at $\{-4, -4, -4\}$. If not possible, explain why.
3. If possible, find a state feedback control so that the closed-loop poles are at $\{-5, -5, -5\}$. If not possible, explain why.
4. if possible, design a state estimator so that the observer poles are at $\{-10, -10, -10\}$. If not, explain why.

AUTOMATIC CONTROL 3 **SPRING 2011**

Consider a negative unity feedback system with plant model

$$P(s) = \frac{1}{(s+1)(s+p)}$$

(a). In the case $p = 6$, design a PI controller so that the steady state error with respect to the unit ramp input is no more than 0.25 and the overshoot is no more than 10%.

(b) For the design in (a), find the crossover frequency ω_c, the phase margin, and the maximum possible steady state error when the reference input is $r(t) = \sin(\omega_c t)$?

(c) For the design in (a), sketch its Nyquist plot.

(d) For the design in (a) with $p \neq 6$, analyze the phase margin for $2 \leq p \leq 5$.

(a) Suppose that $P_n(s) = p_0 s^n + p_1 s^{n-1} + \cdots + p_n$ is Hurwitz and $p_0 > 0$. Use arguments from root locus to show that $P_{n+1}(s) = \delta s^{n+1} + P_n(s)$ is also Hurwitz, provided that $\delta > 0$ is sufficiently small.

(b) Let $G(s) = B(s)/A(s)$, with $B(s)$ Hurwitz, be the plant model and $C(s) = K/s$ be an integrator feedback compensator. Without loss of generality $b_0 > 0$. Show that

$$1 + K\frac{B(s)}{A(s)} = 1 + K\frac{b_0 s^n + b_1 s^{n-1} + \cdots + b_n}{s(s^n + a_1 s^{n-1} + \cdots + a_n)} \neq 0$$

for all s on the closed right half plane provided that $K > 0$ is sufficiently large.

(c) Suppose that $B(s) = (s+1)^2 + 1$ and $A(s) = s^2(s^2 - 4)$. Sketch the root locus in (b) for $K > 0$ without computing the breaking point and $j\omega$-axis crossing.

(d) Suppose in (b) that $b_0 = 0$, $b_1 \neq 0$, and $B(s)$ is Hurwitz. Find the existence condition of the stabilizing gain K in terms of poles and zeros of $G(s)$.

Consider state-space system: $\dot{x}(t) = Ax(t) + Bu(t)$, $x(0) = x_0$, where $x(t) \in \mathbf{R}^n$ and $u(t) \in \mathbf{R}^m$.

(a) Find the solution $x(t)$ for $t \geq 0$.

(b) Show that the system, i.e., (A, B), is controllable, if and only if the controllability Gramian

$$G_c(T_f) = \int_0^{T_f} e^{At} B B^T e^{A^T t} \, dt > 0,$$

for any $T_f > 0$. That is, $G_c(T_f)$ is positive definite.

(c) Suppose that (A, B) is controllable and $x_0 = 0$. For a given $x_f \in \mathbf{R}^n$, find control input such that $x(T_f) = x_f$ where $T_f > 0$. Discuss what will happen for your control input in the case of $T_f \to \infty$.

The transfer function for a causal digital filter is given by $H(z) = \frac{z-b}{z-a} = \sum_{n=0}^{\infty} h_n z^{-n}$, where $|a| < 1$ and $a \neq b$. Both a and b are real numbers.

(a) Use the long division to determine h_n in terms of a and b, $\forall n$.

(b) Use the inverse z-transform by partial fraction expansion to determine h_n in terms of a and b, $\forall n$.

(c) Assume $F_L(z) = \sum_{n=0}^{L} h_n z^{-n}$, where L is a positive integer. Define $\rho = \frac{\sum_{n=0}^{L} |h_n|^2}{\sum_{n=0}^{\infty} |h_n|^2}$. Find the algebraic expression for L, in terms of ρ, a, and b.

(d) According to (c), determine the *normalized approximation error* as given by

$$\frac{\int_{-\pi}^{\pi} \left| F_L(e^{j\omega}) - H(e^{j\omega}) \right|^2 d\omega}{\int_{-\pi}^{\pi} \left| H(e^{j\omega}) \right|^2 d\omega},$$

in terms of ρ, where $j = \sqrt{-1}$, $F_L(e^{j\omega}) = \sum_{n=0}^{L} h_n e^{-j\omega n}$, and $H(e^{j\omega}) = \frac{e^{j\omega}-b}{e^{j\omega}-a}$.

White noise with power spectral density $S_X(f) = N_0/2$ is applied to a filter with impulse response $h(t) = 1$ for $0 < t < 1$ and 0 otherwise.

1. Find the cross power spectral density $S_{XY}(f)$.
2. Find the cross-correlation $R_{XY}(\tau)$.
3. Find the output power spectral density $S_Y(f)$.
4. Find the output auto-correlation $R_Y(\tau)$.
5. Find the output power P_Y.

Assume that the Fourier transform of the continuous-time signal $x(t)$ for $t \in (-\infty, +\infty)$ is given by $X(j\omega) = e^{-j\omega}$ for $\omega \in [-1, 1]$ and 0 otherwise.

Let the signal $y(t) = \frac{d^2x(t)}{dt^2}$, the second-order derivative of $x(t)$.

1. Find the Fourier transform of the signal $y(t)$, namely, $Y(j\omega)$.
2. Find the total energy of the signal $y(t)$, namely,
$$\int_{-\infty}^{+\infty} |y(t)|^2 dt.$$
3. Find a signal $z(t)$ such that its Fourier transform is $Z(j\omega) = j\omega Y(j\omega)$.
4. Given the linear system defined by
$$r(t) = \int_0^t x(\tau) d\tau,$$
find the Fourier transform of the output signal $r(t)$, namely, $R(j\omega)$.

Given a deterministic low-pass signal $x(t)$ generated at point A whose Fourier transform is $X(f)$, where $X(f) = 0$ for $|f| > B_w$, and the peak amplitude of $x(t)$ is $X_{max} < \infty$. Consider a remote point C which is interested in restoring $x(t)$.

- Assume the received signal at C is $r(t) = s(t) + w(t)$, where $w(t)$ is an additive white Gaussian noise (AWGN) with power spectral density $N_0/2$ and $s(t)$ is the digitally modulated signal transmitted from A.
- Consider a scalar uniform mid-rise quantizer at A with $L = 2^R$ levels to quantize $x(t)$, where R is the number of bits used to represent each level. (Note: a mid-rise quantizer maps an input to R bits by dividing the entire range of each $x(t)$ uniformly into L (even) levels, and each representing point is the mid point of each quantization cell.)
- Assume an uncoded BPSK modulation with transmission energy E_s and basis function $\phi(t), t \in [0, T]$ is used to transmit digitized information from $x(t)$ through the AWGN channel, where T is the symbol period.

Answer the following questions:

(a) Provide a system block diagram including all processing units at both A and C in order to achieve your goal of recovering $x(t)$ at C.

(b) Can we have $x(t)$ perfectly restored at C? Justify your answer. If not, further remark on the sources of uncertainty, as well as how they contribute to making the restored signal $\hat{x}(t)$ not equal to $x(t)$.

A binary communication system with two equiprobable messages uses the following signals:

$$s_1(t) = \begin{cases} 1 & 0 \le t < 1 \\ 2 & 1 \le t < 2 \\ 0 & \text{otherwise} \end{cases}$$

$$s_2(t) = \begin{cases} 1 & 0 \le t < 1 \\ -2 & 1 \le t < 2 \\ 0 & \text{otherwise} \end{cases}$$

1. Find the energy of each of the transmitted signals.
2. Assuming that the channel is additive white Gaussian noise with power spectral density of $N_0/2$ watts/Hz, find the error probability of the optimal receiver (the one that minimizes the probability of error) and express it in terms of N_0.
3. Assume that we have a two-path channel and the two received signals are given by

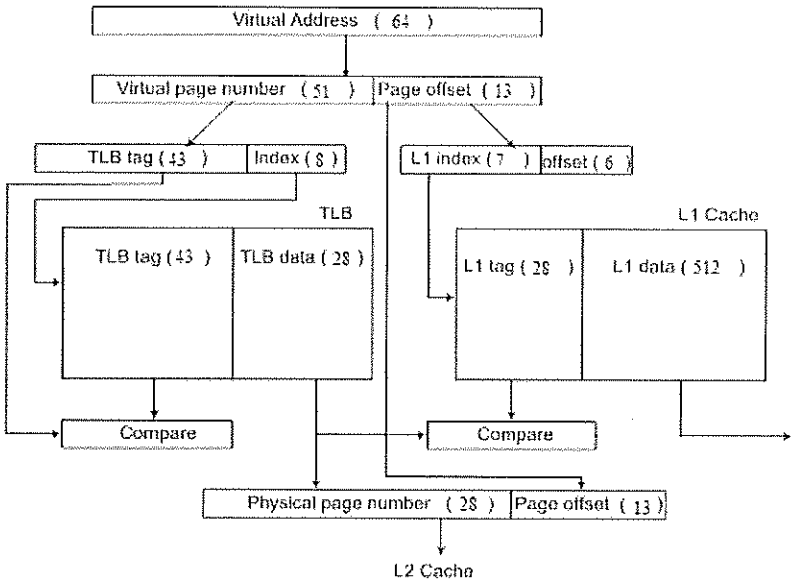
$$r_1(t) = s(t) + N_1(t), \quad r_2(t) = s(t) + N_2(t),$$

where $s(t)$ is the transmitted signal and where $N_1(t)$ and $N_2(t)$ are independent white Gaussian noise processes with power spectral density of $N_0/2$ and they are independent of the transmitted message. The receiver makes its decision based on the two received signals $r_1(t)$ and $r_2(t)$. Determine the structure of the optimum receiver and find its probability of error.

4. Now suppose that

$$r_1(t) = As(t) + N_1(t), \quad r_2(t) = s(t) + N_2(t),$$

where A is a constant known to the receiver. In this case what is the receiver's optimal decision rule?



The overall picture of a hypothetical memory hierarchy going from virtual address to L2 cache access is shown above. The page size is 8KB. The TLB is direct mapped with 256 entries. The L1 cache size is 32KB with 4-way set-associative design with 64-byte blocks. The virtual address is 64 bits and the physical address is 41 bits. The number of bits for each item is denoted. For example, virtual address (64) means the virtual address has 64 bits.

A. Describe the procedure of a L1 data cache access illustrated by the above figure in details.

B. In the above cache accessing procedure, can the TLB and the L1 cache be searched in parallel? You must justify your answer in details.

C. Suppose the L1 cache size increases from 32KB to 128KB and other parameters remain unchanged. Can the TLB and the L1 cache be searched in parallel? If yes, answer the reason clearly; if not, state your reason and propose a solution to make this parallel search possible.

The ***test-and-set*** spin lock is the simplest synchronization mechanism possible on most commercial shared-memory machines. This spin lock relies on the exchange primitive to atomically load the old value and store a new value. The lock routine performs the exchange operation repeatedly until it finds the lock unlocked (i.e., the returned value is 0).

```
tas:     ADDI    R2, R0, #1
lockit:  EXCH    R2, 0(R1)    //Atomic exchange value of R2 and memory 0(R1)
         BNEZ    R2, lockit
         ......
```

Unlocking a spin lock simply requires a store of the value 0.

```
unlock:  SW      R0, 0(R1)
```

The more optimized ***test-and-test-and-set*** lock uses a load to check the lock, allowing it to spin with a shared variable in the cache.

```
tatas:   LD      R2, 0(R1)
         BNEZ    R2, tatas
         ADDI    R2, R0, #1
         EXCH    R2, 0(R1)
         BNEZ    R2, tatas
```

Now consider a bus-based, symmetric shared memory system with 4 processors. Each processor has its own cache. Assume that processors P0, P1, and P2 are all trying to acquire a lock at address 0x100 (i.e., register R1 holds the value 0x100). The stall cycles resulting from processor operations are listed in the following table.

Operation	Stall Cycles
CPU read/write misses if satisfied by the memory.	100
CPU read/write misses if satisfied by a remote cache.	50
CPU write hits and generate an invalidation.	15

In the following questions, we have these assumptions: (1) the critical sections are 1000 cycles long; (2) the processors acquire the lock in the order of P0, P1 and P2; (3) the cache block containing the address 0x100 only has a valid copy in memory initially.

a. Using the ***test-and-set*** spin lock, determine how many memory stall cycles each processor incurs before acquiring the lock.
b. Using the ***test-and-test-and-set*** spin lock, determine how many memory stall cycles each processor incurs before acquiring the lock.
c. How many bus transactions occur for each lock respectively?

Computer Hardware 5 **Fall 2011**

Considering the following MIPS-like code:

```
1.  LW    R1, 100(R2)   // R1 ← [100+R2]
2.  ADD   R3, R1, R8    // R3 ← R1+R8
3.  LW    R5, 10(R3)    // R5 ← [10+R3]
4.  AND   R8, R3, R6    // R8 ← R3 && R6
5.  SUB   R4, R5, R7    // R4 ← R5 - R7
6.  XOR   R3, R1, R9    // R3 ← R1 ⊕ R9
```

(a) Consider a processor with a single issue, in-order seven stage pipeline: instruction fetch (F), instruction decode / register read (D), execution / effective address generation (X), memory access stage 1, 2 and 3 (M1, M2 and M3), write-back (W). Assume that there are three forwarding paths to each of the ALU input: (1) the ALU output at the beginning of the M1 stage, (2) the ALU output at the beginning of the W stage and (3) the memory output at the beginning of the W stage. Complete the pipeline diagram showing the execution of the code on the processor. You answer should be in the format of the following table. Denote pipeline stalls with a "-".

Instruction	1	2	3	4	5	6	7	8	...	...	...
1. LW R1, 100(R2)	F	D	X	M1	M2	M3	W				
2. ADD R3, R1, R8											
3. LW R5, 10(R3)											
4. AND R8, R3, R6											
5. SUB R4, R5, R7											
6. XOR R3, R1, R9											

(b) Assume the processor from part (a) is enhanced with load value prediction hardware. With this scheme, load instructions can speculatively obtain their values after the instruction fetch (F) stage. Therefore the load dependent instructions can execute with the speculative value smoothly and the pipeline doesn't stall. At the beginning of the load's WB stage, the processor will check between the true data value fetched from memory and the speculative value. For the above code, if the first load instruction (instruction 1) gets the ***wrong*** value from the prediction hardware and the second load instruction (instruction 3) gets the ***correct*** value, complete the pipeline diagram showing the execution of the code. Please devise a reasonable recovery method and show its operation in the diagram. You need pay attention to avoid the structural hazard. You also must use the format in part (a).

Computer Software 1. **Fall 2011**

a) Let a,b,m be positive integers where $m \neq 1$. Prove that $(a + b)modm = (amodm + bmodm)\ modm$.

b) Let c,m be positive integers where m $\neq 1$. The multiplicative inverse $modm$ of the number c, denoted as $c^{-1}\ modm$, is an integer e such that $(c \times e)modm = 1$.

Let (c,m) denote the greatest common divisor of c and m.

Prove that if $(c,m) = d \neq 1$, then $c^{-1}\ modm$ does not exist.

Hint: Provide a proof by contradiction in this part b).

Consider a directed acyclic graph $G = (V, E)$ that represents dependencies among a set of tasks. Each vertex in G corresponds to a task, and each edge $(u, v) \in E$ indicates that task u must complete before v can start. The graph is represented in an adjacency list form.

(a) Assume that the execution time (or, delay) of the tasks is one unit of time. Derive an efficient sequential algorithm that computes all the pairs of nodes that can never be executing at the same time. Explain why your algorithm is correct. What is the time complexity of your algorithm, in terms of the number of edges and number of vertices? Show all the steps in your derivation of the time complexity.

(b) For this part, assume that the execution time (or, delay) each task i is t_i where t_i is an integer and $t_i \geq 1$. Derive an efficient sequential algorithm that computes all the pairs of nodes that can never be executing at the same time. Explain why your algorithm is correct. What is the time complexity of your algorithm, in terms of the number of edges and number of vertices? Show all the steps in your derivation of the time complexity.

There is a flight of stairs with n steps. You can climb 1, 2 or 3 steps in one stride. Let t_n denote the number of different ways in which you can climb the n-step flight of stairs.

For example, $t_3 = 4$ with the four different methods of climbing the stairs being $\langle 3 \rangle$, $\langle 1, 2 \rangle$, $\langle 2, 1 \rangle$, $\langle 1, 1, 1 \rangle$; here $\langle 1, 2 \rangle$ represents climbing the first step separately, and the last two steps in one stride. In $\langle 1, 1, 1 \rangle$, each step is climbed separately.

Your answers to all the questions below must be justified.

(a) Determine t_1, t_2 and t_4; it is given that $t_3 = 4$.

(b) Construct a recurrence relation for t_n, for any $n \geq 1$.

(c) Consider a string of symbols. These symbols are represented in binary and have variable length. They are drawn from the set $\{0, 10, 110, 111\}$. Thus each string of x symbols has a length ℓ (in bits) that satisfies $x \leq \ell \leq 3x$. Derive a recurrence relation for T_n, the number of distinct n-bit strings.

(d) Given an n-bit string, outline an efficient algorithm to identify the symbols in the string.

(e) What are the difficulties posed in constructing an algorithm as in part (d), if the symbols are drawn from the set $\{0, 1, 10, 110, 111\}$?

A *perfect shuffle* of a list of $2n$ quantities $x_0, x_1, \cdots, x_{2n-1}$ is the permutation

$$x_0, x_n, x_1, x_{n+1}, x_2, x_{n+2}, \cdots, x_{n-1}, x_{2n-1}$$

We will use this definition later in this problem.

For integers $n \geq 0$ and let $\alpha \geq 0$ be a multiple of 2^{2n}. Let $A(n)$ be a $2^n \times 2^n$ array of points, numbered from α to $\alpha + 2^{2n} - 1$. A renumbering of $\{\alpha, \alpha+1, \alpha+2, \cdots, \alpha+2^{2n}-1\}$ is defined to be a *2-D filling function* for $A(n)$ as follows. Divide $A(n)$ into four quadrants $A_0(n-1)$, $A_1(n-1)$, $A_2(n-1)$ and $A_3(n-1)$, each a $2^{n-1} \times 2^{n-1}$ sub-array of A. For a 2-D filling function

- the (new 2-D filling function) numbers of $A(n)$ must be distinct,
- the new numbers within any of the $A_i(n-1)$'s (for $0 \leq i < 4$) must be from an interval of $2^{2(n-1)}$ contiguous integers, and
- each of the $A_i(n-1)$'s must be (recursively) numbered by a 2-D filling function.

(a) What is the perfect shuffle of a, b, c, d, e, f, g, h?

(b) Which of the following numberings of a 4×4 array is a 2-D filling function? Justify your answer.

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

(i)

0	1	2	3
7	6	5	4
8	9	10	11
15	14	13	12

(ii)

0	1	4	5
2	3	6	7
8	9	12	13
10	11	14	15

(iii)

(c) Consider $A(n)$, a $2^n \times 2^n$ array of points where the element in row i and column j is indexed $i2^n + j$; here $0 \leq i, j < 2^n$. This is called the row-major indexing of (i, j). Define the *shuffled row-major* index of (i, j) to be the number obtained by a perfect shuffle of the $2n$-bit binary representation of the row-major index of (i, j). Specifically, if the binary representation of the row major index of (i, j) is $x_0 x_1 \cdots x_{2n-1}$, then the binary representation of the shuffled row major index is.

$$x_0 x_n x_1 x_{n+1} x_2 x_{n+2} \cdots x_{n-1} x_{2n-1}$$

Construct the shuffled row-major indexing for a 4×4 array.

(d) Prove that the shuffled row-major indexing for a $2^n \times 2^n$ array is a 2-D filling function.

Suppose we use a triangle mesh to represent a 3D object (see Figure 1), then we can discretely measure the shape on the mesh. Suppose we have stored the mesh in a graph: each vertex is a node, associated with its (x, y, z) coordinates, and each edge corresponds a path connecting nodes.

For example, given two vertices $\mathbf{p}_1$, $\mathbf{p}_2$,

$$\mathbf{p}_1 = \begin{pmatrix} x_1 \\ y_1 \\ z_1 \end{pmatrix}, \mathbf{p}_2 = \begin{pmatrix} x_2 \\ y_2 \\ z_2 \end{pmatrix},$$

the Euclidean distance between them is simply $|\mathbf{p}_1\mathbf{p}_2| = |\mathbf{p}_2 - \mathbf{p}_1|$.

(a) We usually want to compute the *geodesic curve* between two points, i.e., the path with the shortest length that traverses over the surface. This path can be discretely approximated on the mesh (graph) as $\{\mathbf{p}_1, \mathbf{p}_2, \mathbf{p}_3, \ldots, \mathbf{p}_n\}$, composed of consecutive edges $[\mathbf{p}_i, \mathbf{p}_{i+1}], i = 1, \ldots, n-1$, (each $\mathbf{p}_i$ is a vertex). Given two vertices, describe your algorithm to find this approximate path and compute its curve length.

(b) What is the area of a triangle $[\mathbf{p}_i, \mathbf{p}_j, \mathbf{p}_k]$? What is the approximate area of the model's surface?

(c) How to compute the volume of a tetrahedron $[\mathbf{p}_i, \mathbf{p}_j, \mathbf{p}_k, \mathbf{p}_l]$?

(d) Suppose a given surface ∂M is the boundary of a solid object M. You have the discrete triangle mesh representation of ∂M, can you compute the volume of M? Please discuss the generality of your algorithm, and show whether it works for all kinds of geometry. Try to develop a robust and general algorithm.

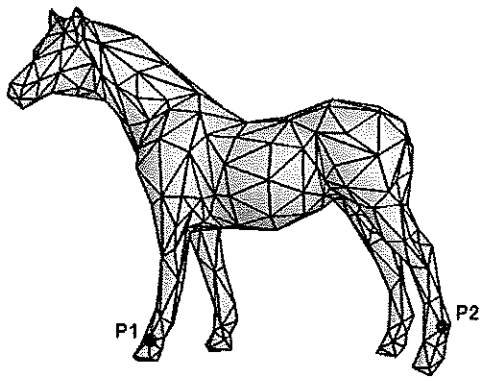


Figure 1: A triangle mesh.

(a) Given two points $\mathbf{p}_1, \mathbf{p}_2$ on the E^2 plane, the *cross product* $\mathbf{p}_1 \times \mathbf{p}_2$ can be used to detect that with respect to the origin $\mathbf{q}(0,0)$, whether $\mathbf{qp}_1 = (x_1, y_1)$ is at the clockwise (CW) or counterclockwise (CCW) side (about the origin) from $\mathbf{qp}_2 = (x_2, y_2)$. Illustrate the geometric interpretation of the cross product, and explain how to tell this by looking at $\mathbf{p}_1 \times \mathbf{p}_2$.

(b) Based on the routine of (a), can you detect whether two line segments $[\mathbf{p_1}, \mathbf{p_2}]$ and $[\mathbf{p_3}, \mathbf{p_4}]$ are intersected? Write your intersection detection pseudo-code algorithm:
bool $Check(\mathbf{p_1}, \mathbf{p_2}, \mathbf{p_3}, \mathbf{p_4})$,
which takes 2D coordinates $(x_i, y_i), i = 1, 2, 3, 4$ of these points as the input, and returns whether $[\mathbf{p_1}, \mathbf{p_2}]$ intersects $[\mathbf{p_3}, \mathbf{p_4}]$ or not.
Note: (1) assume $[\mathbf{p_1}, \mathbf{p_2}]$ and $[\mathbf{p_3}, \mathbf{p_4}]$ are not collinear; and (2) here you shall only use the routine in (a), i.e. cross product, for this detection.

(c) With $Check()$ operator developed in (b), given a set of n line segments $[\mathbf{p}_i, \mathbf{q}_i], i = 1, \ldots, n$, how to detect whether or not any intersection exists? Can you do it in $O(n^2)$ time? Can you do it in $O(n \log n)$ time?
Hint: you can assume the line segments and their endpoints ($\mathbf{p}_i$,$\mathbf{q}_i$) are sparsely located and are not degenerated: (1) no three endpoints are collinear; (2) no two endpoints locate in the same position; and (3) no three or more segments intersect at a same point.

Computer Application 5 **Fall 2011**

Wavelet transforms are used in image processing to filter the noise or compress the information. Let $X = \left(c_{n,0}, c_{n,1}, \ldots, c_{n,2^j-1}\right)$ be the image data. A simple wavelet transform, called Haar transform, obtains scaling coefficients $c_{j,k}$ and wavelet coefficients $d_{j,k}$ using following equations:

$$\left.\begin{aligned} c_{j,k} &= \frac{c_{j+1,2k} + c_{j+1,2k+1}}{2} \\ d_{j,k} &= \frac{c_{j+1,2k} - c_{j+1,2k+1}}{2} \end{aligned}\right\} \qquad (1)$$

Here j and k identify the k^{th} element at j^{th} level, where $j = n, n - 1, \ldots, 0$ and $k = 0, 1, \ldots 2^j-1$ for data of size 2^n. For $j = n$, $X = \left(c_{j,k}\right)$.

(a) Using (1), obtain Haar transform for data $X = (3, 1, 0, 4, 8, 6, 9, 9)$.

(b) Write equations similar to (1) that will generate X from the result obtained in (a)

(c) Generalize (b) to recreate X from $c_{j,k}$ and $d_{j,k}$ for $j < n$.

(d) Write an efficient algorithm for forward (1) and inverse (c) Haar transforms.

Circuits & Systems
Problem #1

Fall 2011

A BiCMOS amplifier is shown below. Calculate the small-signal voltage gain v_0/v_i.

Assume $I_S = 10^{-16}$ A, $\beta_F = 100$, $r_b = 0$, $V_A \rightarrow \infty$, $\mu_n C_{ox} = 200\ \mu A/V^2$, $V_t = 0.6V$ and $\lambda = 0$.

I_S: Reverse saturation current of the p-n junction

β_F : BJT current gain in forward active mode of operation

r_b : Base resistance of the BJT

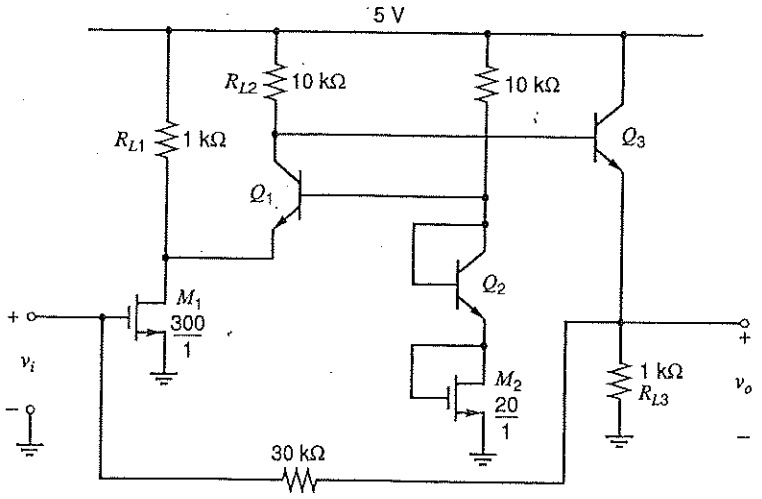
V_A : Early voltage in BJT

$\mu_n C_{ox}$: Process transconductance parameter of MOSFET where μ_n is the mobility of electrons in the channel region and C_{ox} is the gate oxide capacitance per unit area.

V_t : MOSFET threshold voltage

λ : MOSFET channel length modulation parameter

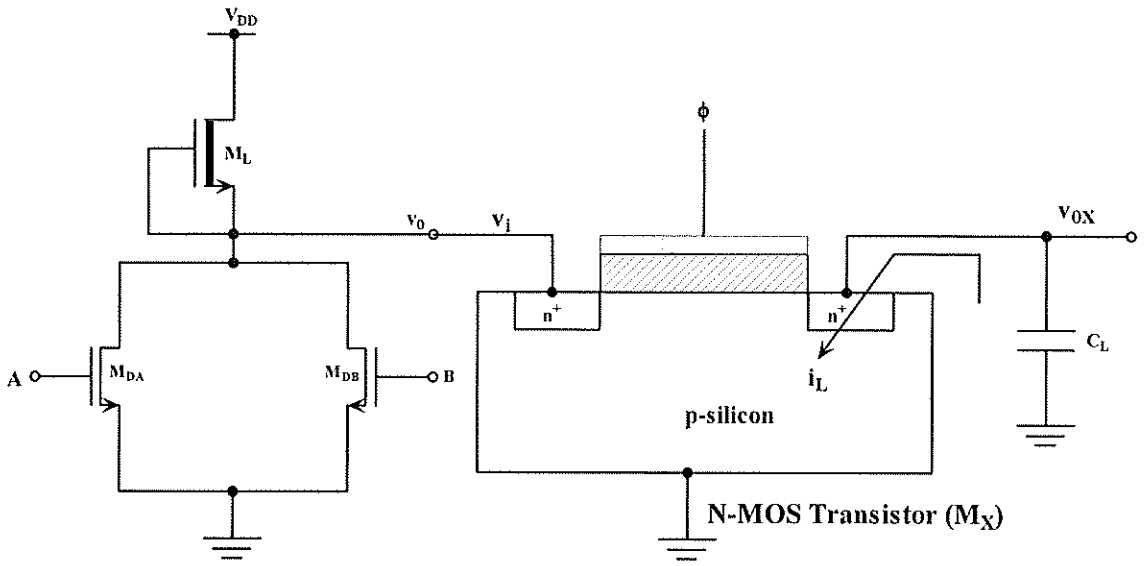
Note: $V_{BE} = 0.7V$.
Assume that the dc input is adjusted so that $I_{C1} = I_{C2}$. I_{C1} and I_{C2} are collector currents of transistors Q_1 and Q_2, respectively.
Use MOSFET I-V equation for the saturation region of operation.



Circuits & Systems
Problem #2

Fall 2011

a) The following circuit is biased at V_{DD} = 5V. Assume that K_N = 35 $\mu A/V^2$. Also assume the width-to-length ratios of the load and driver transistors are $(W/L)_L$ = 1 and $(W/L)_D$ = 4, respectively. Let V_{thD} = 0.8 V and V_{thL} = -2 V. Neglect the body effect and consider n-MOS transistor (M_X) is off. Determine the low output voltage of the circuit when A = logic 1 (5 V) and B = Logic 0 (0 V), and when both inputs are high (5 V). $K_N = \mu_n C_{ox}$ is the process transconductance parameter. V_{thD} and V_{thL} are threshold voltages of driver and load transistors, respectively.

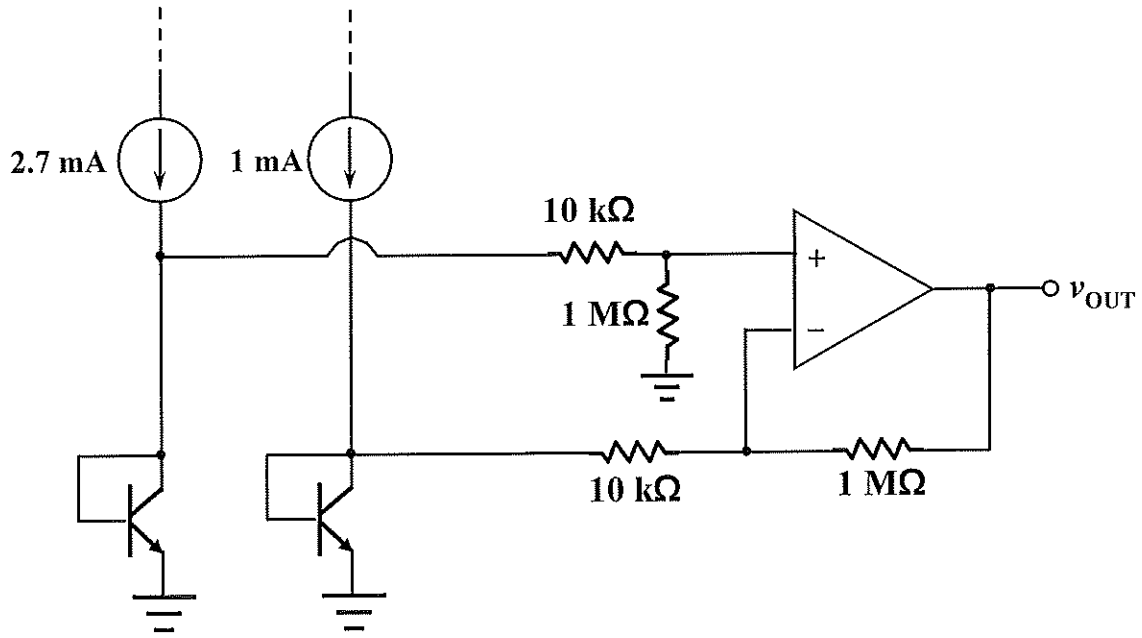


b) Estimate the rate at which the output voltage, V_{0X} decreases with time. Assume the capacitor is initially charged to V_{0X} = 4.2 V. Let C_L = 1 pF and assume the reverse-biased p-n junction leakage current is constant at i_L = 1 nA.

Circuits and Systems
Problem 3

Fall 2011

For an electronic thermometer circuit given below, answer the following questions.



(*a*) Express v_{OUT} in terms of the ambient temperature T. Assume that the two transistors in the circuit are identical.

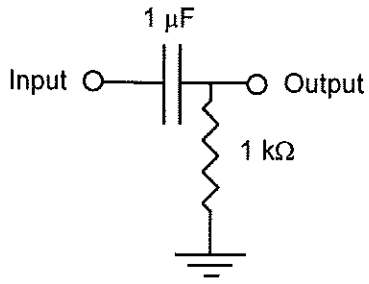
(*b*) Discuss about the limit of the circuit.

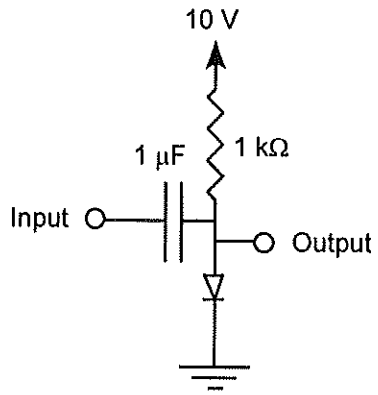
Circuits and Systems
Problem 4

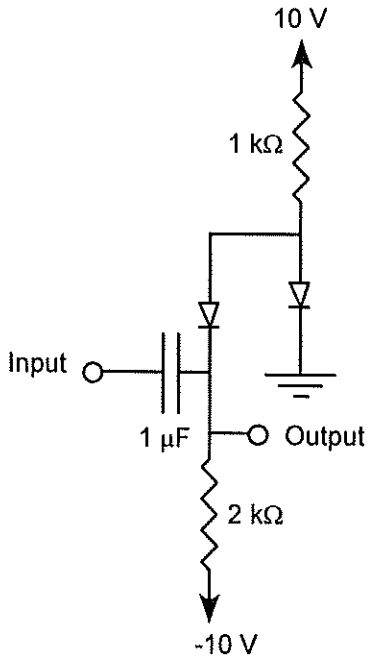
Fall 2011

A 10 Volt p-p square wave at a frequency of 100 Hz is applied to the inputs of each circuit below.

Sketch the output waveforms, clearly indicating times and amplitudes.





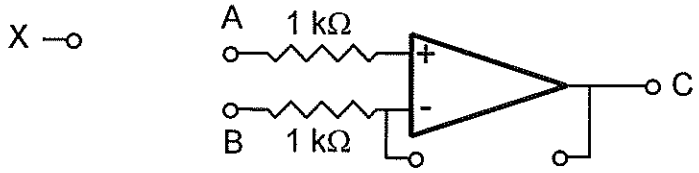


Circuits and Systems Fall 2011

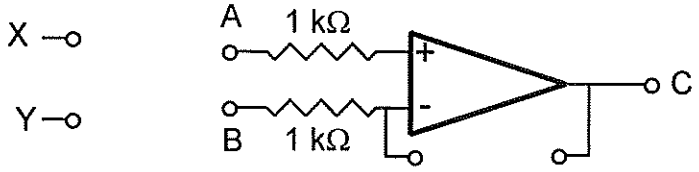
Problem 5

You have two signals, X and Y, both varying between 0 and 1 Volt.

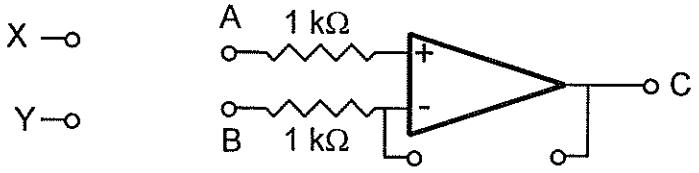
a) Add components to the circuit below so that the output at point C is proportional to the signal at X. Estimate the maximum and minimum values at C.



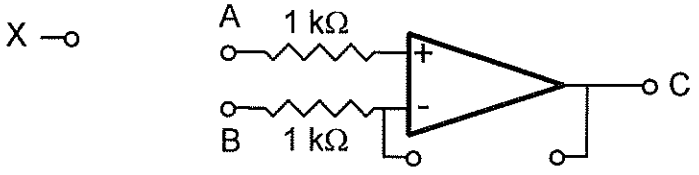
b) Add components to the circuit below so that the output at point C is proportional to the sum of the signals at X and Y. Estimate the maximum and minimum values at C.



c) Add components to the circuit below so that the output at point C is proportional to the difference of the signals at X and Y. Estimate the maximum and minimum values at C.



d) Add components to the circuit below so that the output at point C is proportional to the logarithm of the signal at X. Estimate the maximum and minimum values at C.



Physical Electronics
Problem 3

Fall 2011

1. A p-n junction diode current can be looked upon as net recombination or generation of electron-hole pairs per unit time somewhere inside the diode. Explain the validity of this statement.
2. A forward biased light emitting diode (LED) made from a direct band gap material (band gap = 2.3 eV) draws 4.5 kA/cm^2 current when connected to an external terminal battery voltage of 2.6 V. The diode cross-section area is 90 μm^2. In this semiconductor, 92% of recombinations are known to be radiative. The diode packaging permits 85% of emitted photons to exit from the package, the remaining being absorbed by the packaging material. The LED is made of a p$^+$-n junction i.e. the p-side is much more heavily doped than the n-side.

   For this case, determine:
   a) Number of photons coming out of the LED/sec.
   b) Heat dissipated inside the diode material (in Watts).
   c) Efficiency of the LED to convert electric energy from a battery to externally observable light energy.
   d) Where is most of light generated inside the diode? Explain giving reasons.

State any assumptions made. Magnitude of an electron charge q = 1.6 × 10^{-19} C.

Physical Electronics
Problem 4

Fall 2011

Consider a p-type semiconductor bar of length L in equilibrium with an acceptor impurity density distribution $N_A(x)$, where $0 \leq x \leq L$ is distance along the bar. Assume 100% impurity ionization. $N_A(x) >> n_i$, the intrinsic carrier density for all values of x.

a) If $N_A(x)$ is known to be uniform i.e. constant with distance x along the bar, find the value of equilibrium electric field $E_o(x)$. Show intermediary steps.

b) Repeat part a) above if $N_A(x)$ is now a linear function of x i.e. $N_A(x) = C + D\,x$, where C and D are constants and > 0.

c) Determine $N_A(x)$ if $E_o(x)$ in the material is known to be constant i.e. $E_o(x) = E$, where E is a constant < 0.

d) For part c) above, qualitatively plot equilibrium energy band diagram showing all pertinent energy levels. Label your diagram carefully. Also plot $E_o(x)$ and equilibrium electrostatic potential $V_0(x)$ as a function of x for $0 < x < L$.

e) For part c) above, is the material neutral i.e. is the space charge zero at position x? Explain clearly. Where are the charges that produce the field located?

Physical Electronics
Problem 5

Fall 2011

An n-channel MOSFET with channel width W = 20 μm and channel length L= 1 μm, oxide thickness t_{ox} = 5 nm and uniform substrate doping $N_A = 10^{15}\ cm^{-3}$, is used as a voltage controlled resistor. Neglect body effect. For this device, the current voltage relationship is given by:

$I_D = \frac{W}{L}\mu_n C_{ox}\left[(V_{GS} - V_{Tn})V_{DS} - \frac{V_{DS}^2}{2}\right]$ where I_D is the drain current, μ_n = 550 $cm^2/V.s$ is channel electron mobility, C_{ox} is oxide capacitance per unit area, V_{GS} is gate to source voltage, V_{Tn} is threshold voltage, V_{DS} is drain to source voltage. kT/q = 26 mV where k is Boltzmann constant and T is absolute temperature, $q = 1.6 \times 10^{-19}\ C$ is magnitude of electron charge and intrinsic carrier density $n_i = 1.5 \times 10^{10}\ cm^{-3}$. Relative permittivity of oxide ε_{ox} = 3.9 and permittivity of free space $\varepsilon_o = 8.854 \times 10^{-14}\ F/cm$.

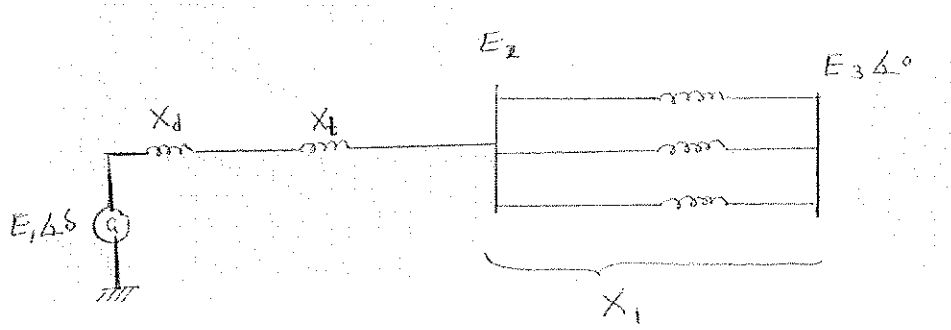
Depletion width $d = \sqrt{\frac{2\varepsilon_{rs}\varepsilon_o\phi_s}{qN_A}}$ where relative permittivity of silicon ε_{rs} = 11.8 and ϕ_s is silicon surface potential.

For this device, determine the following stating any assumptions made:

a) Calculate the inversion layer charge density (in C/cm^2) required for the MOSFET to act as a 2.5 $k\Omega$ resistor between the source and the drain terminals at very low values of V_{DS}. What is the corresponding number density of charge carriers (number/cm^2)? Show all the intermediary steps.
b) Calculate the value of V_{GS} in excess of V_{Tn} required to obtain the inversion charge density in part a) above.
c) Compute the depletion charge density at on-set of strong inversion in this device and compare it to the inversion charge density in part a) above.
d) From the results of part c) above, can you justify neglecting the inversion charge density while calculating the value of threshold voltage V_{Tn}? A qualitative explanation is required.

POWER 1 **FALL 2011**

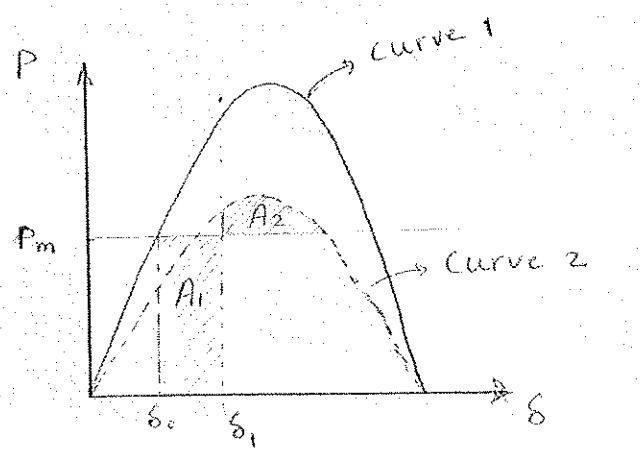
The synchronous generator shown in the following figure is connected to infinite bus E_3 through the generator stator reactance X_d, transformer reactance X_t, and transmission line impedance X_1. The generator is modeled using the classical model (with constant internal voltage E_1.) The generator is delivering active power P_0 under the internal voltage $E_1\angle\delta_0$ where $\delta_0 = 30^0$. At time t=0 a symmetric three-phase fault with zero impedance occurs at bus 2 between the generator bus and the infinite bus.



1- What changes occur to the delivered power by the generator to the grid immediately after the fault?

2- Suppose that the fault lasts for t_1 seconds. What changes occur to the generator angular speed ω ?

3- Suppose that curve 1 in the graph shown below represents the variation of active power as a function of δ before the fault has occurred where P_m is the input mechanical power from turbine and δ_0 is the generator internal voltage angle prior to the fault. When the fault is removed at t_1 resulting in the generator's angle δ_1, one of the parallel transmission lines are dropped resulting in the variation of after-fault active power P_2 as a function of δ shown in curve 2. Neglecting the stator and transformer reactances, find the maximum available power $P_{2\max}$ as a function of P_m.



4- In Part 3, assume that $P_{2\max}$ is greater than P_m, what can be said about the areas A1 and A2 if the generator is stable after the fault removal.

Figure 1. shows PWM inverter applied as a compensator.

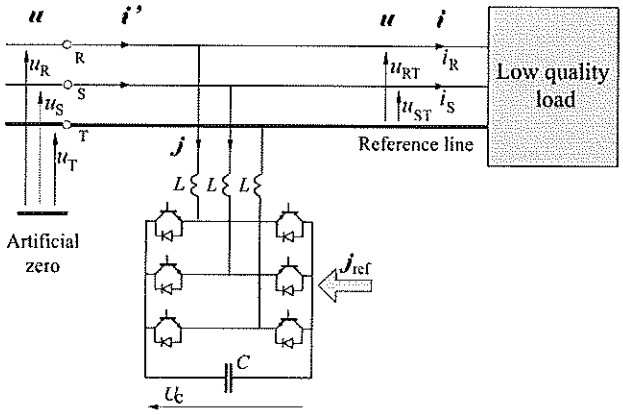


Fig.1

Develop formula for the reference signal j_{ref} if the compensator is to reduce:

A. The load reactive current,

B. The load unbalanced current,

C. The load current harmonics.

A. Explain how commutation notches and spikes, as shown in Fig. 2, occur in three-phase AC/DC converters.

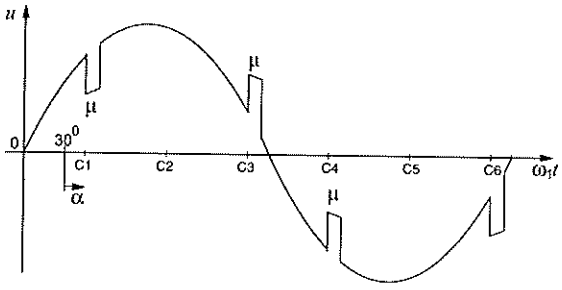


Fig. 2

B. Develop formula for calculating commutation angle μ.

C. Develop formula for calculating the voltage harmonics caused by commutation.

POWER 4 **Fall 2011**

1) Draw the equivalent circuit of a single-phase transformer. What kind of measurements have to be done to determine the parameters of this circuit?

2) Draw the phasor diagrams of currents and voltages, one for the inductive and one for pure resistive load. Show when the voltage regulation is greater.

3) A single phase transformer built (in Europe) for the rated frequency of 50 Hz is going to be connected to the power line (in US) of rated voltage and 60 Hz frequency. Will the power losses in the transformer increase or decrease with respect to those at 50 Hz frequency (assuming the transformer is loaded by the rated current in both circumstances). Explain what kind of power losses and why.

4) 3 single-phase transformers of the turn ratio 10:5 are connected to the 3 phase line of 220 V line voltage. Their primary and secondary windings are connected, first both in Δ and next both in Y.
    - Draw the circuit diagrams for both cases
    - What are the secondary phase voltage and the line voltage in each of the two connections?

Power 5 **Fall 2011**

1) What are the differences in a design between 3-phase induction slip-ring motor and squirrel cage motor? Which one of these two motors would you recommend to drive the fan and which to drive a long fully loaded belt conveyer? Explain why.

2) Draw the equivalent circuit of induction motor without core losses parameter and show where the mechanical power and stator and rotor winding losses dissipate. What is the mechanical output power at zero speed and at synchronous speed?

3) What are the similarities in the operation of induction motor and transformer? In which of these two machines the no-load current is greater (related to their rated currents)? Explain why.

4) If you could vary the supply parameters (voltage and frequency) what would you do to change the speed of induction motor to keep the constant electromagnetic torque? Use torque-speed characteristic to explain.

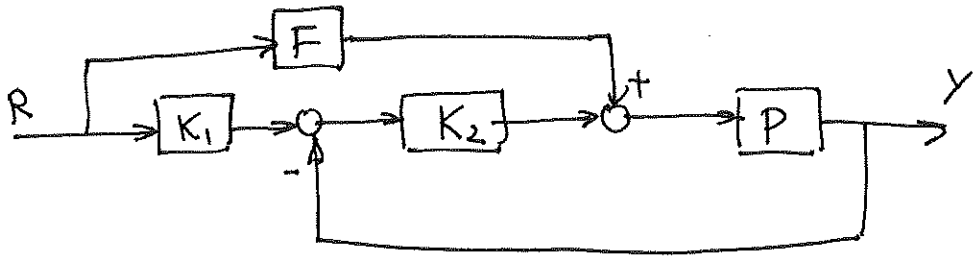
Let a unity feedback system with a plant model be given by

$$G(s) = \frac{K(\tau s + 1)}{s(s+1)(Ts+1)}.$$

1. Sketch Nyquist diagrams for $\tau > T > 0$ and $T > \tau > 0$ respectively.
2. Using Nyquist stability criterion, find the stability condition of the system.
3. Using Nyquist stability criterion, find the relationship between τ and T so that the system is stable for every $K > 0$.

AUTOMATIC CONTROL 2 **FALL 2011**

Let a feedback control system be shown below



1. Find the transfer function from R to Y.
2. Let
$$P(s) = \frac{10}{s(s+1)}, \quad K_2(s) = \frac{2(s+1)}{s+2}$$
find constants F and K_1 so that the steady state error with respect to a ramp $R(t) = t$ is zero.
3. Can you find constants F and K_1 so that the steady state error with respect to $R(t) = \sin t$ is zero?

Consider a unity negative feedback system with loop transfer function

$$GH(s) = \frac{K(s+1)(\alpha s+\beta)}{s^2(s-1)}.$$

(a) Sketch its Nyquist plot for the case $\alpha = 0$ and $\beta = 1$.

(b) Suppose that $\alpha > 0$ $\beta > 0$. Use Routh-Hurwitz method to determine the stability range of K as a function of α and β.

(c) What is the Nyquist plot for the case $\alpha = 1$ and $\beta = 10$?

A causal linear and time-invariant (LTI) system has the frequency response

$$H(j\omega) = \frac{4 + j\omega}{6 + 5j\omega - \omega^2},$$

where $j = \sqrt{-1}$.

1. Determine a differential equation relating the input $x(t)$ and output $y(t)$ of the above LTI system.
2. Find the output $y(t)$ of the above LTI system when the input is

   $$x(t) = te^{-t}u(t),$$

   where $u(t)$ is the unit-step signal defind as 1 for $t > 0$ and 0 otherwise.
3. Let $Y(j\omega)$ be the Fourier transform of the signal $y(t)$. Find a signal $z(t)$ such that its Fourier transform is $Z(j\omega) = j\omega Y(j\omega)$.

A causal linear-time-invariant system with *initial rest* ($y[n] = 0$, for $n < 0$) is described by a difference equation:

$$y[n] = a_0 x[n] + a_1 x[n-1] + b_1 y[n-1] + b_2 y[n-2],$$

where a_0, a_1, b_1, and b_2 are all real numbers. The z-transforms for $x[n]$, $y[n]$ are denoted by $X(z)$, $Y(z)$, respectively.

1. Determine the transfer function $H(z) = \frac{Y(z)}{X(z)}$ and the associated region of convergence (ROC) in terms of b_1 and b_2.
2. Specify the condition in terms of b_1 and b_2 for the discrete-time Fourier transform (DTFT) $H(e^{j\omega})$ to exist, where $j = \sqrt{-1}$. Then, determine $H(e^{j\omega})$ directly from the result in Part 1.
3. Given $x[n] = \begin{cases} 1, & n = 0, \\ 0, & \text{otherwise} \end{cases}$, $y[4] = 1$, and $y[5] = 2$, find the relationship among a_0, a_1, b_1, and b_2. Then, determine the algebraic formula of $y[n]$, for $n > 5$, in terms of n, a_0, a_1, b_1, and b_2.
4. Determine the z-transform $Y(z)$ for the result in Part 3. Based on $Y(z)$, write the condition for $y[n]$ to be a *sinusoidal* signal as $n \to \infty$.

Consider two real jointly wide sense stationary (WSS) random processes $a(t)$ and $b(t)$ with zero mean and auto-correlation function $R_{aa}(\tau) = E[a(t+\tau)a(t)]$ and $R_{bb}(\tau) = E[b(t+\tau)b(t)]$, respectively, and cross-correlation function $R_{ab}(\tau) = E[a(t+\tau)b(t)]$.

1. For a process $x(t) = a(t)\cos(\omega_0 t) - b(t)\sin(\omega_0 t)$, compute its mean $E(x(t))$ and auto-correlation function $E[x(t+\tau)x(t)]$, where $\omega_0 > 0$ is a given deterministic frequency.
2. Is $x(t)$ a WSS random process? If Not, provide conditions on $R_{aa}(\tau)$, $R_{bb}(\tau)$ and $R_{ab}(\tau)$ under which $x(t)$ is a WSS process.
3. Under the same conditions as obtained in (2) compute the auto-correlation function of $y(t) = a(t)\sin(\omega_0 t) + b(t)\cos(\omega_0 t)$, as well as the cross-correlation function of $R_{xy}(t+\tau, t) = E[x(t+\tau)y(t)]$.
4. We form two complex random processes: $w(t) = a(t) + jb(t)$ and $z(t) = x(t) + jy(t)$, where $j = \sqrt{-1}$. Show that $S_z(f) = S_w(f + f_0)$, where $S_z(f)$ and $S_w(f)$ are power spectral density functions of $w(t)$ and $z(t)$, respectively, and $f_0 = \frac{\omega_0}{2\pi}$.

Consider a binary communication system between node A and node B, where the received signal at B is $Y = W_0$ when node A sends bit 0, and $Y = S + W_1$ when node A sends bit 1 to B. Here, W_j denotes the received noise at B when bit $j \in \{0, 1\}$ is transmitted, whose probability distribution function (PDF) is given by $P_{W_j}(w)$, and $S > 0$ is a positive random variable with PDF $P_S(x)$ and independent of W_j. Let $\pi_j = \Pr(j)$ denote the prior probability of bit $j \in \{0, 1\}$.

1. To minimize the average probability of error $P_e = \Pr(j \neq \hat{j})$, where $\hat{j} \in \{0, 1\}$ denotes the detected bit at B given Y, what is the corresponding decision rule (in terms of a function of Y)?
2. If W_j is Gaussian distributed with zero mean and σ_j^2 variance, and $S > 0$ is a deterministic variable, simplify your decision rule.
3. Under the decision rule in (2), is it possible to have $\alpha + \beta = 1$, where $\alpha = \Pr(\hat{j} = 1|j = 0)$ and $\beta = \Pr(\hat{j} = 0|j = 1)$, justify your answer.

An equally likely binary message is transmitted across an additive white Gaussian noise (AWGN) channel with power spectral density of $N_0/2$ Watts/Hz using the following signal set.

$$\begin{cases} s_0(t) = 0 & 0 \le t < T \\ s_1(t) = \sqrt{\frac{E}{T}} & 0 \le t < T \end{cases}$$

1. Find the probability of error for the optimal receiver (that which minimizes the probability of error).
2. The following demodulator is used in the receiver.

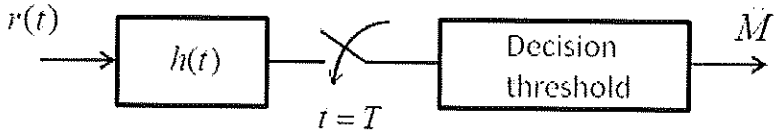


Figure 1: Demodulator

where

$$h(t) = \begin{cases} e^{-At} & 0 \le t < T \\ 0 & \text{otherwise.} \end{cases}$$

(a) Find the threshold in the decision threshold block that minimizes the probability of error.

(b) Find the probability of error for this demodulator.

(c) Evaluate the increase of transmitted energy required so that this receiver achieves the same error probability as the optimal receiver.