

Department of Electrical & Computer Engineering Seminar/Workshop

Power Integrity: A Nanoscale VLSI Challenge

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ABSTRACT

Silicon scaling, an economic backbone of the semiconductor industry, has brought about not only extreme levels of electronic integration, but also significant barriers such as the “Power Wall”, leakage, and in the nanoscale regimes, a significant challenge in Power Integrity. As entire systems are integrated onto nanoscale (sub-100nm) silicon chips, system-level, frequency-domain, 'analog' design and verification aspects are becoming increasingly important, particularly in nanoscale SoC design. Power Integrity analysis in SoC's is hence moving from traditional IR Drop to *total power integrity*, and *true-electromagnetic simulations*, comprehending all aspects of interactions between integrated circuit blocks and the common power delivery network. In this brief discourse, circuit and system techniques applicable to overcome scaling-related challenges are reviewed. Tools and verification methodology advances addressing power integrity in nanoscale silicon design are also discussed.

Date: Thursday, Oct. 2, 2008

Time: 10 AM – noon (Tentative)

Seminar and Q/A: 10 – 11:15 AM followed by Panel Discussions

Panelists: Mr. Raj Nair, Dr. Ashok Srivastava, Dr. Suresh Rai and Dr. Lu Peng

Place: 145-149 Electrical Engineering Building

Brief Vita: Raj Nair obtained his MSEE from Louisiana State University in 1995. He is currently an expert consultant in IC power delivery and power integrity and co-founder of [Anasim](http://www.anasim.com/) Corp. developing and marketing a power integrity aware VLSI floor planner. Prior to Anasim, he founded ComLSI, Inc. that develops and licenses patents and silicon IP in advanced power delivery as well as high-speed signaling. Formerly, he was with Intel Corp. for 7 years, where he led strategic technology path-finding activities in microprocessor packaging, conceived and implemented distributed on-chip voltage regulation in microcontrollers and championed a fully integrated CMOS voltage regulator microprocessor power delivery solution. He holds 40 issued patents, has authored or co-authored numerous conference and journal publications, and has applied many of his inventions to commercial products.

Everyone is invited to attend