3rd Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW-3)

Feb 26th 2012, New Orleans, Louisiana, USA
Held in conjunction with HPCA-18
http://www.ece.lsu.edu/hpca-18/shaw-3/

Organizing Chairs

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Important dates

Abstract/Paper submission
Dec 16 2011, 23:59 PST

Author Notification
Jan 9 2012

Final Paper Submission
Jan 27 2012

Workshop
Feb 26th 2012

New Orleans, Louisiana, USA

February 26th 2012

SHAW-3 Call For Papers

Computing platforms are getting smaller (e.g. handheld devices), richer (e.g. visual computing applications) and broader (i.e. reaching the masses via smartphones and other embedded devices). This trend is made possible by System-on-Chip (SoC) and Heterogeneous Architectures that combine wider power/performance scaling, combinations of high performance and ultra-low power general-purpose cores along with a wide spectrum of domain-specific accelerators or Intellectual Property (IP) blocks. With the recent introduction of general-purpose compute cores such as Intel® Core2 and Atom™ processors, these heterogeneous platforms have the potential to run a much broader range of applications than ever before. The goal of this workshop is to bring together academic researchers and industry practitioners to discuss future SoC and Heterogeneous architectures, Accelerators and Workloads. The research challenges in SoC/Heterogeneous platforms are multi-fold: (a) providing rich functionality and wider power/performance range (b) attempting to cover a broad range of applications that can be migrated from mainstream platforms to SoCs and Heterogeneous devices, (c) enabling a modular architecture and design environment that improves time-to-market and (d) providing a rich software programming environment that eases the challenge of developing applications on a heterogeneous architecture consisting of general-purpose cores as well as specialized accelerators.

Below is the proposed list of topics for the workshop. Topics include, but are not restricted to, the following:

- Novel SoC/Hetero Architectures
  - Different levels of Heterogeneity
  - Heterogeneity in Cores, Frequency, Cache, Memory
  - Power, Performance, Energy optimizations
  - SoCs, CPU/GPU, CPU/GPGPU architectures
  - Adaptive heterogeneity
  - Ultra-Low Power Core Micro-architectures
  - Fabrics / Network-on-chip
  - Cache/Memory Hierarchies
  - HW Support for Heterogeneity
  - HW Support for Programmability
  - HW Support for Modularity
  - Simulation / Emulation Methodologies
- Emerging Workloads and Embedded Devices
  - New Workloads (e.g. Visual computing examples such as Augmented Reality, Multi-modal interfaces, etc)
  - Emerging embedded applications, devices and novel uses cases
  - Workload Analysis for power/performance/energy optimization and acceleration
  - Workload Partitioning between Heterogeneous Cores and Accelerators
  - Performance Monitoring and Simulation
  - Case Studies of SoC/Heterogeneous applications
- Novel Accelerator Designs
  - Specialized Accelerator Architectures and Designs
  - Domain-Specific Programmable/Configurable Accelerators
  - Accelerator Interfaces for Programmability
  - Development Environments for Accelerator Design
  - System-Level integration of Accelerators

Submission Guidelines: Interested authors are encouraged to submit extended abstracts (1 - 2 pages) or short papers (6 pages) by email to the organizing chairs (Ravi Iyer, Ramesh Illikkal and Raj Yavatkar). The deadline for submission is December 16th. Final (short) papers will be due on Jan 27th, 2012 and will be printed in a workshop proceedings made available to the workshop attendees

Note: Best papers from SHAW-3 will be also considered for subsequent publication in IEEE Computer Architecture Letters. More information on this will be available later.