COMPUTER ARCHITECTURE: A QUANTITATIVE APPROACH, SECOND EDITION

ERRATA FOR FIRST AND SECOND PRINTINGS*

END PAPERS, FOREWORD, PREFACE, ACKNOWLEDGMENTS

No.	Page Number	Error
1.	–	In the end papers in the "Rules of Thumb" section, in subpoint 4, replace "quadrupling in three years" with "quadrupling in just over three years"
2.	–	On the copyright page, under "INSTRUCTOR SUPPORT," delete ",ext. 230"
3.	–	On the copyright page, under "INSTRUCTOR SUPPORT," change "http://mkp.com" to "http://www.mkp.com"
4.	**xviii**	Lines 8 and 19, change "http://mkp.com" to "http://www.mkp.com"
5.	–	In the end papers in the "Hardware Description Notation" table, in the "Example" column only, change all instances of "`R1`" to "`Regs[ R1]`", all the instances of "`R2`" to "`Regs[ R2]`", and all the instances of "`R3`" to "`Regs[ R3]`"

* All line numbers refer to running text and do not include tables, figures or code samples.

CHAPTER 1

No.	Page Number	Error
1.	**1**	In the Table of Contents for Chapter 1, change the number for the 2nd entry to "1.2", and the title to "The Task of a Computer Designer," and the page number to "3"
2.	**12**	In the answer to the example, change the final fraction in the "Dies per wafer" equation to $\frac{62.8}{2.12}$, and change "107" to "110"
3.	**26**	Figure 1.12, in the "Arithmetic mean for W(2)" row, change "91.82" to "91.91"
4.	**30**	In the answer to the example, replace the final equation $$\text{Speedup}_{\text{overall}} = \frac{1}{0.6 + \frac{0.4}{10}} = \frac{1}{0.64} = 1.56$$ with $$\text{Speedup}_{\text{overall}} = \frac{1}{0.6 + \frac{0.4}{10}} = \frac{1}{0.604} = 1.66$$
5.	**31**	In the answer to the example, replace the final equation $$\text{Speedup}_{\text{FP}} = \frac{1}{(1 - 0.2) + \frac{0.2}{10}} = \frac{1}{0.82} = 1.22$$ with $$\text{Speedup}_{\text{FP}} = \frac{1}{(1 - 0.2) + \frac{0.2}{10}} = \frac{1}{0.802} = 1.25$$
6.	**34**	In the answer, change the 2nd instance of "$\text{CPI}_{\text{new FPSQR}}$" in the second equation to "$\text{CPI}_{\text{of new FPSQR}}$"
7.	**34**	In the answer, replace the final equation $$\text{Speedup}_{\text{new FP}} = \frac{\text{CPUtime}_{\text{original}}}{\text{CPUtime}_{\text{new FPSQR}}}$$ with $$\text{Speedup}_{\text{new FP}} = \frac{\text{CPUtime}_{\text{original}}}{\text{CPUtime}_{\text{new FP}}}$$
8.	**55**	Line 4-5, replace "In the same time period as ENIAC, Howard Aiken was building an electromechanical computer called the Mark-I at Harvard."

with

"In the same time period as ENIAC, Howard Aiken was designing an electromechanical computer called the Mark-I at Harvard, which was built by a team of engineers from IBM."

9. **65** Figure 1.24, in the "Geometric mean" row, change "188" to "187"

10. **65** Exercise 1.12, in subpoint c, replace

"Assume for some benchmark, the fraction of use is 20%"

with

"Assume for some benchmark, the fraction of use is 15%"

CHAPTER 2

No.	Page Number	Error
1.	**80**	Figure 2.10, at the end of the figure caption text, add the following sentence: "Graphics instructions typically operate on many smaller data items in parallel; for example, performing eight 8-bit additions on two 64-bit operands."
2.	**82**	Line 39, replace "The data in Figure 2.9" with "The data in Figure 2.8"
3.	**101**	Figure 2.23, change the row beginning with "`ADD`" so that it reads `SUB  SUB R1,R2,R3  Add  Regs[ R1] <-- Regs[ R2] -Regs[ R3]`
4.	**102**	Figure 2.24, in the row for "`JAL`", replace "`R31<--PC+4;`" with "`Regs[ R31] <-- PC+4;`"
5.	**105**	Figure 2.26, in the "Integer average" column, change the value in the "compare" row to "14%", the value in the "load imm" row to "4%", and the value in the "cond. branch" row to "17%"
6.	**105**	Figure 2.26, change "uncond branch" to "jump"
7.	**106**	Figure 2.27, change "uncond branch" to "jump"
8.	**113**	Lines 24-25, replace "in 1964 for use with the IBM 360" with "in the early 1960s"
9.	**113**	Line 26, replace "of the instruction set" with "of the IBM 360 instruction set"
10.	**120**	Exercise 2.3, in the sentence ending, "...write the best equivalent assembly language code for the high-level-language fragments given." change "fragments" to "fragment"
11.	**121**	Exercise 2.6, delete the last sentence and add the following new sentence: "Assume that values in registers are lost between iterations of the loop."
12.	**121**	Exercise 2.8, replace "the value of i and the address of the array" with "the value of i, the value of `C`, and the address of the array"

CHAPTER 3

No.	Page Number	Error

1.	**128**	In the 2nd code segment, replace
		
		`ALUOutput <-- A op B;`
		
		with
		
		`ALUOutput <-- A func B;`

2.	**129**	Subpoint 5, in the last line, change "opcode" to "function code"

3.	**136**	Figure 3.5, in the 2nd line of code in the "IF" row, replace
		
		`IF/ID.NPC, PC <-- (if EX/MEM.cond {EX/MEM.NPC} else {PC+4});`
		
		with
		
		`IF/ID.NPC, PC <-- (if EX/MEM.cond {EX/MEM.ALUOutput} else {PC+4});`

4.	**136**	Figure 3.5, in the 3rd line of code in the "EX" row, replace `ID/EX.A op ID/EX.B;`" with "`ID/EX.A func ID/EX.B;`"
5.	**138**	In the answer to the example, replace Average instruction execution time = 10 + 7 + 10 + 10 + 7 with Average instruction execution time = 10 + 8 + 10 + 10 + 7
6.	**145**	In the example, after "but no pipelining for this instruction," insert "(meaning that the next time instructions could not use the result or be a multiply without incurring a stall)"
7.	**145**	In the answer to the example, in the 4th line from the bottom of the page, replace "and 14% of the instructions take 5 cycles each." with "and 14% of the instructions take 6 cycles each (one normal cycle plus five stall cycles)."
8.	**152**	In the 1st line of the table, replace "`SW R1, 0(R2)`" with "`SW 0(R1), R2`"
9.	**155**	Line 6, change "(B)" to "(C)"
10.	**155**	Figure 3.15, in the 2nd sentence of the figure caption text, replace "from the ALU directly" with "from MEM/WB directly"

11. **158** Line 2, replace “a load source” with “the source instruction being a load”

12. **158** Figure 3.18, replace the “Matching operand fields” column with the following,

ID/EX.IR $_{11..15}$ = = IF/ID.IR $_{6..10}$

ID/EX.IR $_{11..15}$ = = IF/ID.IR $_{11..15}$

ID/EX.IR $_{11..15}$ = = IF/ID.IR $_{6..10}$

13. **159** Line 15, replace “All forwarding happens” with “All forwarding logically happens”

14. **163** Figure 3.22, make the following changes:

The control line for the Mux in the first pipeline stage should come directly from the Zero? test, rather than from ID/EX. Likewise, the top input to the Mux in the first pipeline stage should come directly from the ADD box in the second pipeline stage (ID), rather than from the ID/EX.

15. **163** Line 1, before the sentence beginning “Figure 3.23...” insert the following new sentence:

“Although this reduces the branch delay to one cycle, it means that an ALU instruction followed by a branch on the result of the instruction will incur a data hazard stall.”

16. **163** Line 2, replace “from Figure 3.3 (page 133)” with “from Figure 3.5 (page 136)”

17. **164** Figure 3.23, in the 2nd line of code in the “IF” row, replace

```
IF/ID.NPC,PC <-- (if ID/EX.cond {ID/EX.NPC} else {PC+4});
```

with

IF/ID.NPC,PC <-- (if(Regs[IF/ID.IR$_{6..10}$ op 0){NPC+(IR$_{16}$)^{16}} ## IR$_{16...31}$} else {PC+4});

18. **164** Figure 3.23, in the “ID” row, delete the 2nd line of code; in the 3rd line of code in that row insert a semicolon after “`ID/EX.IR <-- IF/ID.IR`” and delete the rest of that line

19. **166** Line 7, replace “the predictions are” with “the actions for a branch are”

20. **166** Line 8, delete “and the predictions are compile time guesses.” Before the sentence beginning “After discussing...” insert the following new sentence:

“The software can try to minimize the branch penalty using knowledge of the hardware scheme and of branch behavior.”

21. **167** Lines 10-11, replace “scheme is to predict the branch” with “scheme is to treat every branch”

22. **168** Line 1, replace “is to predict the branch” with “is to treat every branch”

23. **169** Figure 3.23, in the 3rd box in the top row, move the line “SUB R4, R5, R6” down so that the arrow in the box points to that line of code

24. **171** Figure 3.31,

In the “doduc” row, change “8%” to “7%” and change “41%” to “40%”

In the “hydro2d” row, change “16%” to “17%”

In the “mdljdp2” row, change “8%” to “9%” in both instances

In the “FP average” row, change “FP average” to “**FP average**”, “34%” to “33%”, and “9%” to “10%”

In the “**Overall average**” row, change “11%” to “12%”

25. **173** Figure 3.33, replace the “Delayed branch” row with the following:

Delayed branch 0.35 0.25 0.0 0.30 0.21 1.06 1.03

26. **174** In the answer to the example, replace

“These frequencies for the SPEC integer programs are 4%, 10%, and 6%, respectively.”

with

“These frequencies for the 10 SPEC programs are 4%, 6%, and 10%, respectively.”

27. **174** Figure 3.35, in the “Frequency of event” row, change “10%” to “6%” and change “6%” to “10%”

28. **175** In the code segment, replace the line “....” with “`ADD R10,R4,R3`”

29. **181** In subpoint 4, replace “instructions are always synchronous” with “instructions are usually synchronous”

30. **181** Point 4, after the sentence ending “...be stopped and restarted.” insert the following new sentence:

“Asynchronous exceptions that occur within instructions arise from catastrophic situations (hardware malfunction, e.g.) and always cause program termination.”

31. **189** Figure 3.43, last row, change the latency value from “24” to “14” and the initiation interval value from “24” to “15”

32. **190** Figure 3.44, caption, in the 2nd line of the figure caption text, replace “requires 25 clock cycles” with “requires 15 clock cycles”

33. **190** Figure 3.45, in the figure caption text, delete the sentence beginning “The FP store...” and add the following new sentence: “FP loads and stores use a 64-bit path to memory so that the pipelining timing is just an integer load or store.”

34. **192** Figure 3.46, replace original figure with the following:

	Clock cycle number																
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LD F4, 0(R2)	IF	ID	EX		WB												
MULTD F0 F4, F6		IF	ID	stall	M1	M2	M3	M4	M5	M6	M7	MEM	WB				
ADDD F2 F0, F8					IF	ID	stall	stall	stall	stall	stall	A1	A2	A3	A4	MEM	
SD 0(R2), F2							IF	ID	EX	stall	stall	stall	stall	stall	stall	stall	MEM

35. **192** Figure 3.46, caption, delete the sentence beginning “Notice that the store...” and insert the following new sentences:

“The SD must be stalled an extra cycle so that its MEM does not conflict with the ADDD. Extra hardware could easily handle this case.”

36. **193** Lines 2-3, replace “enter the MEM stage” with “enter either the MEM or WB stage”

37. **193** Line 7, replace “entrance of the MEM stage” with “entrance of the MEM or WB stage”

38. **193** Line 11, after “...the pipeline.” insert the following new sentence:

“Likewise, stalling before WB would cause MEM to back p.”

39. **197** Line 13, change “column” to “bar”

40. **205** Figure 3.56, in the “Divide” row, replace

U,A,R,D^{28},D+A,D+R,D+R,D+A,D+R,A,R

with

U,A,R,D^{28},D+A,D+R,D+A,D+R,A,R

41. **208** Figure 3.61, reduce the height of the 1st segment of “compress” from 1.25 to 1.0

42. **214** Exercise 3.1, replace “`SW R1,0(R2)`” with “`SW 0(R2)R1`”

43 **217** Line 9, after “...the last two columns.” insert the following sentence:

“Be careful to consider forwarding across an intervening instructions, e.g.,

```
ADD R1, ...
any instruction
ADD ..., R1, ...
```
”

45. **217** Exercise 3.6, change “[15]” to “[20]”

46. **217** Exercise 3.6, after “...to the table in Figure 3.19” insert the following:

“Hint: Remember the tricky case:

```
ADD R1, ...
any instruction
SW ..., R1
```

How is the forwarding handled for this case?”

CHAPTER 4

No.	Page Number	Error
1.	**222**	Line 1, replace "To begin, recall the equation from the last chapter:" with "The CPI of a pipelined machine is the sum of the base CPI and all contributions from stalls:"
2.	**222**	Line 2, replace "The *ideal pipeline CPI* is the maximum throughput attainable" with "The *ideal pipeline CPI* is a measure of the maximum performance attainable"

3.	**225**	In the answer to the example, in the 1st code segment, replace
		
		`SUBI  R1,R1,#8    7`
		`BNEZ  R1,LOOP     8`
		`stall             9`
		
		with
		
		`SUBI        R1,R1,#8    7`
		`stall                   8`
		`BNEZ        R1,Loop     9`
		`stall                   10`

4.	**225**	In the answer to the example, replace "This requires 9 clock cycles per iteration: one stall for the `LD`, two for the `ADDD`, and one for the delayed branch. We can schedule the loop to obtain" with "This requires 10 clock cycles per iteration: one stall for the `LD`, two for the `ADDD`, one for the `SUBI` (since a branch reads the operand in `ID`), and one for the delayed branch. We can schedule the loop to obtain only one stall:"

5.	**225**	In the answer to the example, in the 2nd code segment, replace
		
		`LD          F0,0(R1)`
		`stall`
		`ADDD        F4,F0,F2`
		`SUBI        R1,R1,#8`
		`BNEZ        R1,LOOP     ; delayed branch`
		`SD          8(R1),F4    ; altered and interchanged`
		`                          with SUBI`
		
		with

```
LD          F0,0(R1)
SUBI        R1,R1,#8
ADDD        F4,F0,F2
stall
BNEZ        R1,Loop     ; delayed branch
SD          8(R1),F4    ; altered and interchanged
                          with SUBI
```

6. **225** In the answer to the example, replace

"Execution time has been reduced from 9 clock cycles to 6."

with

"Execution time has been reduced from 10 clock cycles to 6. The stall after ADDD is for the use by the SD."

7. **226** Line 5, after the sentence ending "...clock cycle count for this loop." insert the following new sentence:

"This chain must take at least 6 cycles because of dependencies and pipeline latencies."

8. **226** In the answer to the example, in the last line of code, change "LOOP" to "Loop"

9. **227** In the answer to the example at the top of the page, replace

"This loop will run in 27 clock cycles—each LD takes 2 clock cycles, each ADDD 3, the branch 2, and all the other instructions 1—or 6.8 clock cycles for each of the four elements."

with

"This loop will run in 28 clock cycles—each LD has one stall; each ADDD 2, the SUBI 1, the branch 1, plus 14 instruction issue cycles—or 7 clock cycles for each of the four elements."

10. **227** In the answer to the example, in the last 4 lines of the Loop schedule replace

```
SD          -16(R1),F12
SUBI        R1,R1,#32
BNEZ        R1,LOOP
SD          8(R1),F16;8-32 = -24
```

with

```
SUBI        R1,R1,#32
SD          -16(R1),F12
BNEZ        R1,Loop
SD          8(R1),F16;8-32 = -24
```

11. **228** In the last sentence on the page, replace "with 6.8 cycles" with "with 7 cycles"

12. **230** Lines 16-18, delete from "BNEZ, but this dependence" to the end of the next sentence. Insert the following new text:

"BNEZ; this dependence causes a stall because we moved the branch test for the DLX pipeline to the ID stage. Had the branch test stayed in EX, this dependence would not cause a stall. (Of course, the branch delay would then still be 2 cycles, rather than 1.)"

13. **233** In the 2nd Loop schedule, in the line "`ADDD F8,F6,F2`," add an arrow from "`F8`" to "`F8`" on the following line.

14. **250** In the "Read operands" row, insert the following after "`RK <-- No`":

```
; Qj <-- 0; Qk <-- 0
```

15. **253** Figure 4.8, in the horizontal line that contains 5 connecting dots, remove the 3rd dot

16. **254** In subpoint 3, replace "any functional units waiting" with "any reservation stations waiting"

17. **257** Line 25, change "`MULTD`" to "`DIVD`"

18. **259** Figure 4.11, in the 3rd line of code in the "Issue" row, remove the "`]`" after "`S1`"

19. **261** Figure 4.12, in the 2nd table, change the title of the 3rd column from "**Fm**" to "**Op**"

20. **267** In the 1st code sample, replace

```
L1:   SUBI  R3,R1,#2
```

with

```
L1:   SUBI  R3,R2,#2
```

21. **268** Figure 4.18, replace the "T/NT" row

T/NT	Not taken	Taken

with

T/NT	Taken	Not taken

22. **270** In the answer to the example, replace "$20 \times 2 \times 4K = 8K$" with "$2^0 \times 2 \times 4K = 8K$"

23. **271** In the answer to the example on the preceding page, replace "$22 \times 2 \times 16 = 128$ bits" with "$2^2 \times 2 \times 16 = 128$ bits"

24. **271** In the answer to the example on the preceding page, replace "$22 \times 2 \times$ Number of prediction entries selected by the branch = 8K" with "$2^2 \times 2 \times$ Number of prediction entries selected by the branch = 8K"

25. **274** In the answer to the example, replace

"+ (1 - Percent buffer hit rate $\times$ Taken branches $\times$ 2)"

with

"+ (1 - Percent buffer hit rate) $\times$ Taken branches $\times$ 2"

26. **275** Figure 4.23, in the box at the top of the figure, replace "Send PO to memory" with "Send PC to memory"

27. **275** Figure 4.23, in the left box in the bottom section, replace "Enter branch IO" with "Enter branch instruction address"

28. **281** Figure 4.27, the 9th and 10th rows in the table, replace

```
SD          -24(R1),F16       9
SUBI        R1,R1,#40         10
```

with

```
SUBI        R1,R1,#40         9
SD          -24(R1),F16       10
```

29. **281** Figure 4.27, in the last row, replace "`SD  -32(R1),F20`" with "`SD  -8(R1),F20`"

30. **283** In the example, after "...the integer instruction is the first instruction." insert the following sentence:

"Assume one integer functional unit and a separate FP functional unit for each operation type."

31. **283** In the answer to the example, delete the sentence beginning "The loop runs in 4 = 7/*n* clock cycles..." and insert the following new sentence:

"The loop runs in 4 clock cycles per result, assuming no stalls are required on loop exit."

32. **284** Figure 4.28, make the following changes to the "Executes at clock-cycle number" and "Writes result at clock-cycle number" columns, and add a new column between them:

Executes at clock-cycle number	**Memory access at clock-cycle number**	**Writes result at clock-cycle number**
2	3	4
4		7
3	6	
4		5
5		
6	7	8
8		11
7	10	
8		9
9		

33. **284** Figure 4.28, in the 3rd and 4th lines of the caption text, delete the words "and more write-back ports, which are needed in cycle 8 in this Example." and insert the following new sentences:

"For `LD` and `SD`, the execution is effective address calculation. We assume one memory pipeline."

34. **285** In the answer to the example, in the 2nd code segment, change "1.28 cycles" to "1.29 cycles"

35. **286** Figure 4.29, in the last row of the table, replace "`SD  -0(R1),F28`" with "`SD 8(R1),F28`"

36. **292** In the answer to the example, in the 1st line of code, replace

```
for (i=1; i=i+1; i<=100)  {
```

with

```
for (i=1; i<=100; i=i+1)  {
```

37. **295** In the answer to the example, replace "`SD 0(R1),F4`" with "`SD 16(R1),F4`" and replace "`LD F0,-16(R1)`" with "`LD F0,0(R1)`"

38. **295** In the answer to the example, delete "fetches two array elements beyond the element count." and insert "and store are separated by offsets of 16 (two iterations),"

39. **303** Figure 4.33, delete the "Power PC" column from the table

40. **305** In the answer to example, change "`BNEZ`" to "`BEQZ`"

41. **305** In the answer to the example, replace "After this statement, A will be in R14." with "After the entire code segment is executed, A will be in R14."

42. **315** Figure 4.36, delete the caption text and replace with the following:

"**Only the `LD` and `MULTD` instructions have committed, although all the others have completed execution**. The remaining instructions will be committed as fast as possible."

43. **317** Figure 4.37, in the "Issue" row, 8th line of code, replace

```
Register ['D'].Qi=b
```

with

```
Register ['D'].Reorder=b
```

44. **317** Figure 4.37, in the "Commit" row, 5th line of code, replace

```
else if Reorder[h].Instruction=Store
```

with

```
else if (Reorder[h].Instruction=Store)
```

45. **321** Replace the equation at the top of the page with the following:

$$2n-2+2n-4+\ldots+2=2\sum_{i=1}^{n-1} i=2\frac{(n-1)n}{2}=n^2-n$$

46. **321** Line 5, change "2352" to "2450"

47. **321** Line 9, after the sentence ending "rather than comparing all instructions." insert the following new sentences:

"Of course, if we serialize the instruction issue, the number of comparisons drops. In particular, this large number of comparisons is only needed to simultaneously issue a group of instructions; it is not necessarily needed if the instructions are overlapped."

48. **327** Figure 4.43, in the 2nd line of the caption text, change "integer" to "FP"

49. **327** Figure 4.43, after the sentence ending "issue width of 64 instructions." insert the following new sentence:

"Recall that DLX supplies 31 integer and 16 FP registers, which is the base number provided under 'None.'"

50. **328** Figure 4.44, extend the first bar labeled "12" so that its length is equal to that of the next two bars.

51. **332** Figure 4.48, change the legend text so that it reads as follows:

Infinite 256 128 64
32 16 8 4

52. **335** Line 8, after the sentence ending "Alpha 21164 and UltraSPARC." insert the following new sentences:

"The PowerPC 620 and 604 are very similar. The 604 implements only the 32-bit instruction set and provides fewer buffers; the overall organization, however, is essentially identical."

53. **336** Figure 4.49, in the 3rd line of the caption text, delete the sentence beginning "The condition register..." and insert the following new sentence:

"The condition register used for branches (see Appendix C for a description of conditional branches in the PowerPC architecture) is a 32-bit register grouped as a set of eight 4-bit fields; the BPU provides an additional 16 rename buffers, each can rename one 4-bit field."

54. **337** At the end of the bulleted text at the top of the page, insert the following new sentences:

"The branch unit allows branches to be evaluated independently of the rest of the instructions. In particular, branches do not take issue slots or cycles in the other functional units. When condition registers are set early enough, conditional branches can be executed in parallel with no additional delay."

55. **337** Lines 10-11, replace "eight extra integer and eight extra FP registers" with "eight extra integer and twelve extra FP registers"

56. **340** Line 28, replace "The goal is a the total number of empty instruction slots that is" with "The goal is that the total number of empty instruction slots is"

57. **340** Line 41, change "CPI" to "IPC" in both instances

58. **344** Line 2, replace "$p \times p^2 \times p^3 \times p^4$" with "$p + p^2 + p^3 + p^4$"

59. **350** Line 5, replace "load-store of FP" with "load-store or FP"

60. **351** Line 22, change "1970s" to "1960s"

61. **351** Line 24, replace "The earliest proposal" with "John Cocke made a subsequent proposal"

62. **351** Line 25, delete "was by John Cocke"

63. **351** Line 26-27, replace "The original design was named America and is described" with "He named the design America; it is described"

64. **359** Figure 4.60, extend the bold rule under the column titles to the end of the table

65. **359** Figure 4.60, in the "MIPS R10000" row, change "1995" to "1996"

66. **359** Figure 4.60, in the figure caption text, after the sentence ending "...since no system has yet shipped." insert the following new sentence:

"Issue structure refers to whether the hardware (dynamic) or compiler (static) is responsible for arranging instructions into issue packets; scheduling similarly describes whether the hardware dynamically schedules instructions or not."

67. **361** In the 3rd reference, change “VLIE” to “VLIW”

68. **363** Exercise 4.3, after “...can be scheduled before the if statement” insert “based on the data references”

69. **364** Exercise 4.9, replace “Assume the counts of functional units and the latencies” with “Assume all functional units are fully pipelined and the latencies”

70. **364** Figure 4.61, delete the “Count” column

71. **364** Figure 4.61, in the figure title, replace “Counts and latencies” with “Latencies”

72. **364** Exercise 4.9, in the 3rd line below Figure 4.61, after “dependent stalls” insert “shown in the above table”

73. **365** Figure 4.62, delete the “Count” column

74. **365** Figure 4.62, in the figure title, replace “Counts and latencies” with “Functional unit latencies”

CHAPTER 5

No.	Page Number	Error
1.	**374**	Figure 5.1, replace the labels on the y axis with the following: 100000 10000 1000 100 10 0.1
2.	**384**	Line 1, delete the line and insert the following: "split is 100%/(100% + 26% + 9%) or about 75% instruction references to (26% + 9%)/100% + 26% + 9%)"
3.	**384**	In the example, replace "a miss costs 50" with "the miss penalty is 50"
4.	**385**	In the answer to the example, in the "Average memory access time" equation, change "Read hit" to "Hit", "Read miss" to "Instruction miss", "Write hit" to "Hit", and "Write miss" to "Data miss"
5.	**390**	In the 4th bullet from the top of the page, replace "The first access to a block is not in the cache" with "The very first access to a block *cannot be* in the cache"
6.	**390**	Line 8, after the sentence ending "...the 'three C's.'" insert the following new sentences: "Figure 5.10 shows the same data graphically. The top graph shows absolute miss rates; the bottom graph plots percentage of all the misses by type of a miss as a function of cache size."
7.	**390**	Delete the last two lines on the page.
8.	**392**	Line 1, delete "a function of cache size."
9.	**395**	In the 3rd equation, change "76" to "72"
10.	**409**	Line 13, after the sentence ending "...*blocking factor."* insert the following new sentence: "(Assume x is initialized to zero.)"
11.	**443**	Line 20, replace "final virtual address" with "final physical address"
12.	**446**	Figure 5.41, on the lower right side of the figure, change "<9>" to "<13>"
13.	**446**	Figure 5.41, in the figure title, replace "21064 TLB during" with "21064 data TLB during"
14.	**455**	Figure 5.45, in the 13th line of the figure caption text, after "...and the offset into it" insert ",respectively."
15.	**462**	Figure 4.57, at the end of the figure caption text add the following new sentence: "While the data TLB has 32 entries, the instruction TLB has just 12."

16. **466** Lines 10-13, delete the sentence beginning “This figure makes clear...” and insert the following new sentence:

“This figure makes clear that the primary performance limits of the superscalar 21064 are instruction stalls, which are due to branch mispredictions, and the other category, which includes data dependencies.”

17. **472** Line 6, replace “system wasn’t up to” with “system TSS wasn’t up to”

18. **472** Line 14, change “GE 635” to “GE 645”

19. **477** In the 2nd to last line of code, change “`sec*1e3`” to “`sec*1e9`”

20. **480** Exercise 5.9, change “<5.2>” to “<5.4>”

21. **480** Exercise 5.10, change “<5.2>” to “<5.6>”

22. **480** Exercise 5.10, in subpoint 1, replace the two equations with the following:

((*a* modulo *c*) + (*b* modulo *c*)) modulo *c* = (*a* + *b*) modulo *c*
((*a* modulo *c*) × (*b* modulo *c*)) modulo *c* = (*a* × *b*) modulo *c*

23. **481** Exercise 5.10, in subpoint 3, replace

$$((a_0 + a_3 + \ldots + a_i) \times 1 + (a_1 + a_4 + \ldots + a_{i+1}) \times 2 + (a_2 + a_5 + \ldots + a_{i+2}) \times 4)$$

with

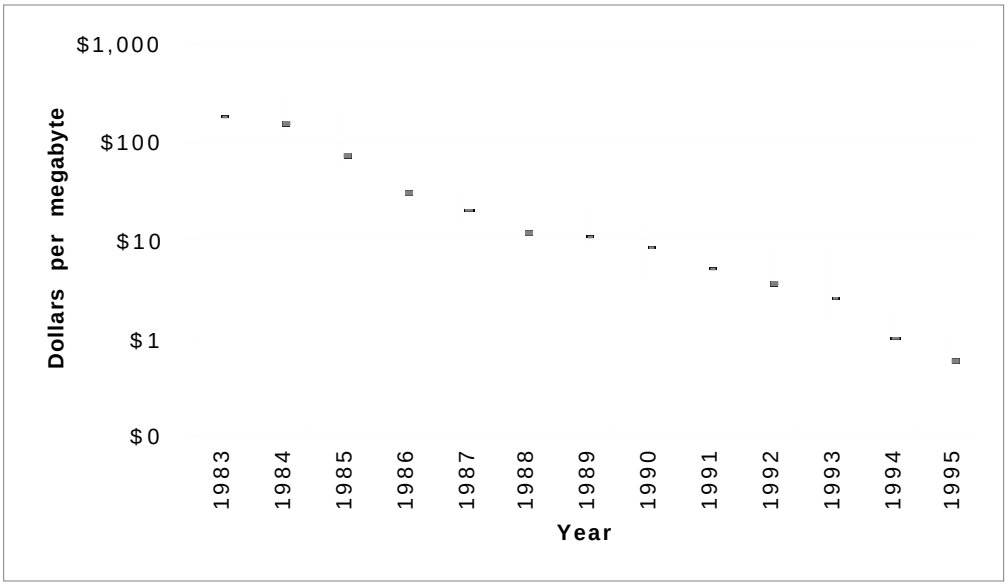
$$((a_0 + a_3 + \ldots) \times 1 + (a_i + a_4 + \ldots) \times 2 + (a_2 + a_5 + \ldots) \times 4)$$

24. **481** Exercise 5.10, in subpoint 3, replace “(*a* sub *j*) = 0, for *j* > *i*” with “$a_j = 0$ for *j* > *i*”

25. **481** Exercise 5.10, in subpoints a and b, change “<5.2>” to “<5.6>”

CHAPTER 6

No.	Page Number	Error
1.	**491**	Figure 6.4, replace existing figure with the following:



2. **516** In the answer to the example, replace

$$5\text{ms} \times \frac{0.1}{1 - 0.1} = 5 \times \frac{0.1}{0.9} = 5 \times 0.11 = 0.55\text{ms}$$

with

$$10\text{ms} \times \frac{0.1}{1 - 0.1} = 10 \times \frac{0.1}{0.9} = 10 \times 0.11 = 1.11\text{ms}$$

3. **516** In the answer to the example, replace "1.27" with "2.56"

4. **516** In the answer to the example, replace "10 + 0.55 ms or 10.55 ms, 2.4 times" with "10 + 1.11 ms or 11.11 ms, 2.25 times"

5. **518** In subpoint 3, replace "coefficient of variance of (C) of one." with "coefficient of variance (C) of one"

6. **520** Figure 6.26, change the "0" on the y axis to "0.1"

7. **532** In the equation for "Maximum IOPS for 25 4-GB disks," change "25 4-GB" to "25 8-GB"

8. **532** In the equation for "Maximum IOPS for 100 1-GB disks," change "100 1-GB" to "100 2-GB"

9. **532** Line 5, change "1500 IOPS" to "1675 IOPS"

10. **532** In the equation for the "Minimum number of SCSI-2 strings for 25 8-GB disks," replace

$$\left\lfloor \frac{25}{15} \right\rfloor$$

with

$$\left\lceil \frac{25}{15} \right\rceil$$

11. **532** In the equation for the "Minimum number of SCSI-2 strings for 100 2-GB disks," replace

$$\left\lfloor \frac{100}{15} \right\rfloor$$

with

$$\left\lceil \frac{100}{15} \right\rceil$$

12. **532** In the equation for "Maximum IOPS for 4 SCSI strings," change "4 SCSI strings" to "2 SCSI-2 strings"

13. **532** In the equation for "Maximum IOPS for 15 SCSI strings," change "15 SCSI strings" to "7 SCSI-2 strings"

14. **534** In the answer to the equation, replace

$$\text{Server utilization} = \frac{\text{Arrival rate}}{\frac{1}{\text{Time}_{\text{server}}/1/(\text{m} \times \text{Time}_{\text{server}})}}$$

with

$$\text{Server utilization} = \frac{\text{Arrival rate}}{\frac{1}{\text{Time}_{\text{server}}/\text{m}}}$$

15. **551** Figure 6.43, in the equation for variable "*b,*" remove the "$\sqrt{\ }$"

16. **558** Exercise 6.5, in every instance, change "TP-1" to "TPS"

17. **558** Exercise 6.5, in subpoint c, after "How fast does a CPU" insert the words "need to be to" and change "100 MB" to "1000 MB"

CHAPTER 7

No.	Page Number	Error
1	**568**	For the bullet points describing *"Transmission time"* and *"Time of flight,"* transpose the order of the bullet points so that the *"Time of flight"* bullet point precedes the *"Transmission time"* bullet point.
2.	**568**	In the *"Transmission time"* bullet point, after "...pass through the network..." insert "...(not including time of flight)..."
3.	**574**	Line 26, change "resorting" to "restoring"
4.	**578**	Line 15, change "error rates" to "cost"
5.	**581**	Figure 7.11, in the figure caption text, change "bits" to "Mbits" in both instances
6.	**582**	In the "Transport $time_{coax}$" equation, change "500×10^6" to "$500/1000 \times 10^6$"
7.	**583**	In the "Transport $time_{tp}$" and "Transport $time_{fiber}$" equations, change "50×10^6" to "$50/1000 \times 10^6$"
8.	**585**	Figure 7.14, delete the figure caption text and replace with the following: "**Figure 7.14 A fat-tree topology for 16 nodes.** The shaded circles are switches and the squares at the bottom are processor-memory nodes. A simple 4-ary tree would only have the links at the front of the figure; that is, the tree with the root labeled 0,0. This three-dimensional view suggests the increase in bandwidth via extra links at each level over a simple tree, so bandwidth between each level of a fat tree is normally constant rather than being reduced by a factor of four as in a 4-ary tree. The multiple paths and random routing gives it the ability to route common patterns well, which ensures no single pattern from a broad class of communication patterns will do badly. In the CM-5 fat-tree implementation, the switches have four downward connections and two or four upward connections; in this figure the switches have two upward connections."
9.	**589**	In the 3rd line of text, replace "node within that is" with "node within that row is"
10.	**602**	Figure 7.21, in the "Peak link BW (MB/sec)" row, replace "Peak link BW (MB/sec)" with "Peak link BW (Mbits/sec)" and change "12" to "155/622"

CHAPTER 8

No.	Page Number	Error
1.	**648**	Line 28, replace "It has an execution time..." with "It has a sequential execution time..."
2.	**652**	Line 14, replace "As" with "For these applications"
3.	**652**	Line 15, replace the phrase "Figure 8.4 shows, as" with "Figure 8.4 shows that as"
4.	**652**	Line 16, after "falls" insert "linearly" and replace "rises, just as we might expect" with "per processor falls more slowly"
5.	**664**	Figure 8.11, in the 5th line of the figure caption text, after the sentence ending "...arc in bold." insert the following new sentences: "The stimulus actions apply to a block in the cache, not to a specific address in the cache. Hence, a read miss to a line in the shared state is a miss for that cache block but for a different address."
6.	**665**	Figure 8.12, on the diagonal line from "Shared" to "Exclusive," replace "Place write miss on bus" with "**Place write miss on bus**". On the diagonal line from "Exclusive" to "Shared," replace "Write-back data; place read miss on bus" with "**Write-back data; place read miss on bus**"
7.	**671**	Lines 1-2, after "a 16-processor run" insert "with a 64-KB cache"
8.	**671**	Figure 8.15, in the figure caption text, delete ", 32-byte blocks,"
9.	**693**	Figure 8.31, in the "Barnes" graph, subdivide the bars into the four sections listed in the legend as follows:

Processor count	Hit	Miss to local memory	Remote miss to home	3-hop miss to remote cache
8	1.0	0.0	0.1	0.1
16	1.0	0.0	0.1	0.1
32	1.0	0.0	0.1	0.1
64	1.0	0.0	0.2	0.1

10.	**701**	Figure 8.34, in the 10th line of the code segment, change "`release=1`" to "`release==1`"
11.	**702**	Figure 8.35, in the 3rd line of the code segment, change "`count++;`" to "`count=count+1;`"
12.	**702**	Figure 8.35, in the 10th line of the code segment, change "`release=local_sense`" to "`release==local_sense`"
13.	**705**	In the code segment, for every line of code that includes two instances of "`*/`", change the 1st instance of "`*/`" to "`/*`".
14.	**705**	In the code segment, delete the ":" in the 4th line of code.
15.	**705**	In the code segment, in the 13th line of code, change "`count++;`" to "`count=count+1;`"

16. **705** In the code segment, in the 23rd line of code, change "=" to "=="

17. **705** In the code segment, in the 27th line of code, change "`|`" to "`!`"

18/ **708** Figure 8.37, in the 8th line of the code segment, change "`release=local_sense`" to "`release==local_sense`"

19. **709** Figure 8.38, change "`A + 0;`" to "`A = 0;`"

20. **711** In the answer to the example, replace "**`sc R2,0(R1)`**" with "**`sc 0(R1), R2`**"

21. **712** In the 1st code segment, in the 3rd line of code, change "`count++;`" to "`count=count+1;`"

22. **712** In the first code segment, in the 10th line of code, change "**`release=1`**" to "**`release==1`**"

23. **717** Figure 8.39, in the "Release consistency" row under the column "Synchronization orderings," change "R-->S_A" to "R-->S_R"

24. **717** Figure 8.40, in the "Release consistency" column, add a line pointing from "`D`" to "`release (S);`"

APPENDIX A

No.	Page Number	Error
1.	**A-15**	Lines 33-34, replace "bits 1 through 9" with "bits 1 through 8"
2.	**A-20**	In the fifth line of the answer to the example, change "A.10" to "A.11"
3.	**A-20**	In the answer to the example, replace the five indented lines with the following reformatted text:

round to $-\infty$	1101_2	add 1 since $r \vee s = 1 \vee 0 =$ TRUE
round to $+\infty$	1102_2	
round to 0	1100_2	
round to nearest	1100_2	no add since $r \vee p_0 = 1 \wedge 0 =$ FALSE
		$r \wedge s = 1 \wedge 0 =$ FALSE

4.	**A-28**	In the equation, change "s^1" to "s_1"
5.	**A-28**	In the equation, change "$e1$" to "e_1" and "$e2$" to "e_2" in each instance
6.	**A-39**	In the last equation, change the last two "0"s so that they are the same size as the first "0"
7.	**A-40**	In the first equation, change p_{1g0} to p_1g_0
8.	**A-40**	In Equations A.8.5 and A.8.6, change the subscripts so that they are all in the smaller font size
9.	**A-42**	Figure A.16, change "j+i" to "j+1"
10.	**A-68**	Line 31, change "Intelís" to "Intel's"
11.	**A-69**	Line 9, change "A.35" to "A.34"

APPENDIX B

No.	Page Number	Error
1	**B-8**	In the answer to the example, in the line that begins with "`SD`" replace "`F4,0(Ry)`" with "`0(Fy)F4`"
2.	**B-14**	Figure B.7, add the following sentences to the end of the figure caption text: "This timing diagram is drawn as if all banks access in clock 0, clock 16, etc. In practice, since the bus allocations needed to return the words are staggered, the actual accesses are often staggered."
3.	**B-18**	In the code segment, replace "`MULTVS  V2,V1,Fs`" with "`MULTSV V2,Fs,V1`"
4.	**B-26**	In the code segment, replace "`sets the VM to 1`" with "`sets VM(i) to 1`"
5.	**B-32**	In the answer to the example, replace $8 \times N_{1/2} = 64$ with $5 \times N_{1/2} = 64$
6.	**B-40**	Lines 26-27, replace "Seymour Cray continues to head the spin-off, which is now called Cray Computer Corporation." with "Seymour Cray headed the spin-off, called Cray Computer Corporation, until its demise in 1995."
7.	**B-40**	Line 40, after the sentence ending "about $1 million." insert the following new sentence: "In mid1995, Silicon Graphics acquired Cray Research, Inc."
8.	**B-44**	Exercise B-3, in subpoint g, change "DLX" to "DLXV"

APPENDIX C

No.	Page Number	Error
1.	**C-4**	Figure C.3, in the "Register-register" format for the SPARC, change "Opx^{11}" to "Opx^{8}"
2.	**C-7**	Figure C.5, in the 1st "Compare" row under "DLX," change "S-" to "S_"
3.	**C-20**	Line 8, change "then" and "if" to "`then`" and "`if`"
4.	**C-24**	Figure C.13, change "IBM ASC 1970" to "IBM ASC 1968"

APPENDIX D

No.	Page Number	Error
1.	**D-24**	In the 2nd line of italics of the first exerpt of italics, change *"performance"* to *"perform"*

APPENDIX E

No.	Page Number	Error
1.	**E-11**	In the heading, change “Directorooy” to “Directory”

REFERENCES

No.	Page Number	Error
1.	**R-13**	In the reference for "Stone, H" replace "*High Performance Computers"* with "*High Performance Computer Architecture"*