Spring 2026 Midterm Exam Review

When / Where

Friday, 20 March 2026 9:30 CDT.

Room 1212 Patrick F. Taylor Hall (where class is held).

Topics

Everything before ISA Families material (`lrisc.s`).

Conditions

Closed Book, Closed Notes

Bring one sheet of notes (both sides), 216 mm × 280 mm.

No use of communication devices...
... even for chats with your LLM BFF.

Format

Several problems, short-answer questions.

Resources

Solved tests and homework:. `https://www.ece.lsu.edu/ee4720/prev.html`

Statically Scheduled MIPS Study Guide:. . .
. . . `https://www.ece.lsu.edu/ee4720/guides/ssched.pdf`

Study Recommendations

Study **this semester's homework assignments**. Similar problems may appear on the exam.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for **brief hints** and **to check** your own solutions.

Emphases

MIPS Programming and Instruction Use

Should be able to write MIPS programs.

Should be able to easily understand MIPS programs.

Should be able to use other ISAs' instructions in examples.

Not required to memorize instruction names, except for common MIPS instructions.

MIPS Implementation

Understand MIPS instruction encoding (the 32 bits starting with opcode).

Implementation Diagrams and Pipeline Execution Diagrams

They are a *team*, so study them together.

RISC-V

Understand RISC-V RV-32i instructions and encoding.

Understand important differences between MIPS and RISC-V.

Topics

ISA v. Implementation.

See Lecture Slides 1—`https://www.ece.lsu.edu/ee4720/2026/lsli01.pdf`

Why separating ISA from implementation is important.

Why it's hard to design an ISA without bias towards first implementation.

MIPS ISA

See MIPS Overview—`https://www.ece.lsu.edu/ee4720/2026/lmips.s.html`

Write and read programs.

Understand how instructions are coded.

Statically Scheduled MIPS Implementations

See Lecture Slides 6—`https://www.ece.lsu.edu/ee4720/2026/lsli06.pdf`
and Statically Scheduled Study Guide—`https://www.ece.lsu.edu/ee4720/guides/ssched.pdf`

Unpipelined Implementation

Understand relationship between insn format and connections to register file, etc.

Pipelined Implementation Versions

Basic (no bypassing).

ALU bypassing, branch in ID.

Many variations covered in class and in assignments.

Terminology

Dependency Definitions

Hazard Definitions

MIPS Implementation Skills

For a Given Pipelined Implementation

Show pipeline execution diagrams.

Remember that...
... the instruction that you are thinking about is in exactly one stage, ...
... stages to the right $\longrightarrow$ have earlier instructions, ...
... and stages to the $\longleftarrow$ left have later instructions.

Show register contents at any cycle.

Design control logic.

Add bypass paths.

Add functional units.

Floating-Point Instructions

See FP Demo Code—`https://www.ece.lsu.edu/ee4720/2026/lfp.s.html`

MIPS Floating Point Instructions.

Arithmetic Instructions

Load and store to FP registers, move-from and move-to instructions.

Format conversion.

Condition-code setting and testing.

RISC-V

Differences Between RISC-V RV-32i and MIPS I

- Branch delay slot.
- Size of immediate in type-I instructions.
- Placement of the destination register field.
- Immediate encoding: Simple ISA or low-cost implementation.

Material in Chapter 2 of the RISC-V specification.

The RV-32i Implementation from Homework 4.