Spring 2025 Midterm Exam Review

When / Where

Friday, 21 March 2025 9:30 CDT.

Room 1212 Patrick F. Taylor Hall (where class is held).

Topics

Everything up to and including floating-point instructions (but not their implementation).

Conditions

Closed Book, Closed Notes

Bring one sheet of notes (both sides), 216 mm × 280 mm.

No use of communication devices.

Format

Several problems, short-answer questions.

Resources

Solved tests and homework:. `https://www.ece.lsu.edu/ee4720/prev.html`

Statically Scheduled MIPS Study Guide:. . .
. . . `https://www.ece.lsu.edu/ee4720/guides/ssched.pdf`

Study Recommendations

Study **this semester's homework assignments**. Similar problems may appear on the exam.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for **brief hints** and **to check** your own solutions.

Emphasis

MIPS Programming and Instruction Use

Should be able to write MIPS programs.

Should be able to easily understand MIPS programs.

Should be able to use other ISAs' instructions in examples.

Not required to memorize instruction names, except for common MIPS instructions.

MIPS Implementation

Implementation Diagrams and Pipeline Execution Diagrams

They are a *team*, so study them together.

Topics

ISA v. Implementation.

See Lecture Slides 1—`https://www.ece.lsu.edu/ee4720/2025/lsli01.pdf`

Why separating ISA from implementation is important.

Why it's hard to design an ISA without bias towards first implementation.

MIPS ISA

See MIPS Overview—`https://www.ece.lsu.edu/ee4720/2025/lmips.s.html`

Write and read programs.

Understand how instructions are coded.

Statically Scheduled MIPS Implementations

See Lecture Slides 6—`https://www.ece.lsu.edu/ee4720/2025/lsli06.pdf`
and Statically Scheduled Study Guide—`https://www.ece.lsu.edu/ee4720/guides/ssched.pdf`

Unpipelined Implementation

Understand relationship between insn format and connections to register file, etc.

Pipelined Implementation Versions

Basic (no bypassing).

ALU bypassing, branch in ID.

Many variations covered in class and in assignments.

Terminology

Dependency Definitions

Hazard Definitions

MIPS Implementation Skills

For a Given Pipelined Implementation

- Show pipeline execution diagrams.
- Show register contents at any cycle.
- **Design control logic**.

Add bypass paths.

Add functional units.

ISA Families: RISC, CISC, VLIW

See ISA Families Overview—`https://www.ece.lsu.edu/ee4720/2025/lrisc.s.html`

Key distinguishing features and their rationale.

RISC: Goal: Easy pipelining, simple (relatively) implementation.

Fixed-length instructions, balanced work, aligned memory access.

CISC: Goal: Powerful instructions, compact code size.

Flexible operand types, multiple-activity instructions.

VLIW: Goal: Easy superscalar implementation.

Bundled instructions, dependence information.

RISC to RISC Differences: MIPS v. SPARC v. RISC-V v. ARM A64

See ISA Families Overview—`https://www.ece.lsu.edu/ee4720/2025/lrisc.s.html`

Opcode fields (and their extensions).

Immediate operands, immediate sizes.

Integer branches.

CISC ISA Features

Goal: Powerful Instructions

Powerful: Many memory addressing modes.

Powerful: Many immediate sizes.

Powerful: Few limits on where addressing modes can be used.

Floating-Point Instructions

See FP Demo Code—`https://www.ece.lsu.edu/ee4720/2025/lfp.s.html`

MIPS Floating Point Instructions.

Arithmetic Instructions

Load and store to FP registers, move-from and move-to instructions.

Format conversion.

Condition-code setting and testing.