LSU EE 4720 **Homework 6** **Due: 23 April 2025**

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Collaboration Rules

Each student is expected to complete his or her own assignment. It is okay to work with other students and to ask questions in order to get ideas on how to solve the problems or how to overcome some obstacle (be it a question of MIPS or assembler syntax, interpreting error messages, how a part of the problem might be solved, etc.) It is also acceptable to seek out assembly language resources for help on MIPS, etc. It is okay to make use of AI LLM tools such as ChatGPT and Copilot to generate sample code. (Do not assume LLM output is correct. Treat LLM output the same way one might treat legal advice given by a lawyer character in a movie: it may sound impressive, but it can range from sage advice to utter nonsense.)

After availing oneself to these resources **each student is expected to be able to complete the assignment alone**. Test questions will be based on homework questions and **the assumed time needed to complete the question will be for a student who had solved the homework assignment on which it was based**.

Student Expectations

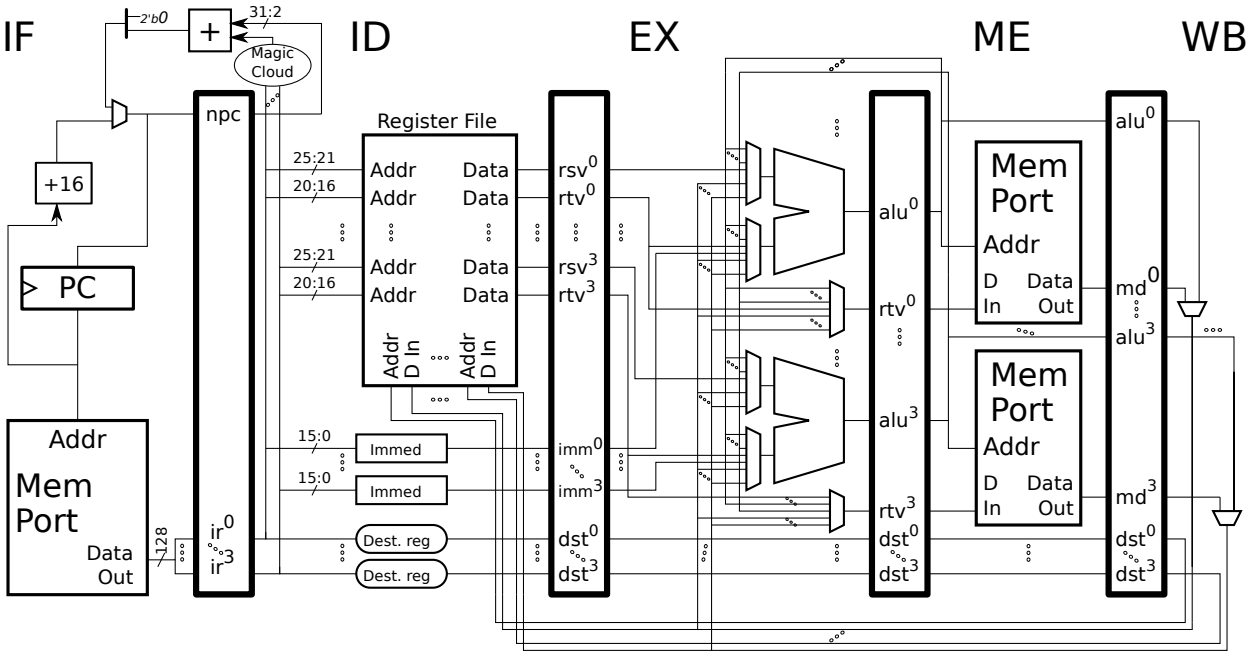
Some of the problems require thought, and students are expected to persevere until they find a solution. It is each student's duty to him or herself to resolve frustrations and roadblocks quickly, hopefully helped along by the satisfaction of making progress. There are plenty of old problems and solutions to look at. One way to resolve issues is to ask Dr. Koppelman or others for help.

Resources

Questions about superscalar MIPS implementations can be found in most final exams.

Problem 1: The following questions are based on 2021 Final Exam Problem 2(c), but **it is not identical**.

(*a*) Appearing below is a 4-way superscalar MIPS implementation which is **slightly different in an important way** from the one appearing in the 2021 Final Exam. In both this implementation and the one on the 2021 exam fetch is not aligned (which makes things easier). Also, there is no branch prediction, which is how we have been doing things in class.



☐ Show the execution of the code below for enough iterations to determine instruction throughout (IPC). (Note: There is no need to put slot numbers on the stage labels.) ☐ Don't forget that it is 4-way superscalar.

```
LOOP:
 lw r10, 0(r1)
 add r3, r10, r3
 sw r3, 0(r5)
 addi r5, r5, 4
 bne r1, r9, LOOP
 addi r1, r1, 4
 lb r8, 0(r9)
 xor r11, r8, r10
```

(*b*) The code from the solution to Final Exam 2021 2(c) has an instruction throughput of $\Theta_c = 0.75\,\text{insn/cycle}$. The solution to part 2(d) did not give the instruction throughput of the solution but did explain that the unrolled code is four times faster.

☐ What is the instruction throughput (IPC) of the 2(d) solution? (The pipeline execution diagram is in the solution, use that!)

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☐ Why can't we use the instruction throughput of parts (c) and (d) to show how much faster part (d) is?

(*c*) In part (d) the loop was to be unrolled degree 2. Here, unroll the loop degree 3 (start with three copies of the loop body) but for the implementation shown here (not from the exam). A correct solution should execute without stalls, but instructions will be squashed due to the branch (which can't be avoided in a 4-way superscalar without branch prediction).

☐ Unroll degree 3 and optimize so there are no stalls.

Problem 2: Solve 2024 Final Exam Problem 2 (all parts), in which code for a 2-way superscalar MIPS implementation is to be completed (a) and the execution of code on a 4-way superscalar MIPS implementation is to be found.