Spring 2024 Final Exam Review

When / Where

Thursday, 9 May 2024 17:30-19:30 (5:30 PM - 7:30 PM) CDT.

Room 1720 Business Education Complex.

Conditions

Closed Book, Closed Notes

Can bring one 215×280 mm note sheet.

Cannot use communication devices.

Format

Two or three or maybe four medium to long problems.

Short-answer questions.

Resources

Check course Web page daily for hints, new resources.

Web page: `https://www.ece.lsu.edu/ee4720/index.html`

RSS feed: `https://www.ece.lsu.edu/ee4720/rss_home.xml`

Solved tests and homework:. `https://www.ece.lsu.edu/ee4720/prev.html`

Study Recommendations

Study homework assigned this semester—**test questions are often based on homework questions.**

Solve **previous test problems**, start with more recent problems.

Memorizing solutions is not the same as solving problems.

Following and understanding solutions is not the same as solving problems.

Use the solutions for brief hints and to check your own solutions.

Emphases

Implementation Diagrams and Pipeline Execution Diagrams

They are a *team*, so study them together.

Designing and analyzing control logic and datapath.

Control Logic

We can't rely on magic performed by others.

Instruction Use

Should be able to easily write MIPS programs.

Should be able to use MIPS instructions in examples.

Not required to memorize instruction names, except for common MIPS instructions.

Topics

Introductory Material

ISA v. Implementation.

fr-5

Instruction Coding.

Fixed-length, variable-length, and bundled instructions.

Splitting of opcode field (as in MIPS type-R instructions).

ISA Classifications: RISC, CISC, VLIW

Dependency Definitions

Hazard Definitions

fr-6

ISA Familiarity

MIPS

Read programs, write programs, implement (design hardware)

SPARC

Read common instructions.

Use of condition codes.

Instruction coding differences.

RISC-V

Instruction coding differences.

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fr-7

MIPS

Classification: RISC

Goals: ISA should allow simple, high-speed implementation.

Instruction types.

Know how to read and write MIPS programs.

fr-8

Statically Scheduled MIPS Implementations

See Lecture Slides 6—`https://www.ece.lsu.edu/ee4720/2024/lsli06.pdf`
and Statically Scheduled Study Guide—`https://www.ece.lsu.edu/ee4720/guides/ssched.pdf`

Pipelined Implementations

Basic (no bypassing, 2-cycle branch penalty), bypassed, branch in ID.

For a Given Pipelined Implementation

Show pipeline execution diagrams.

Show register contents at any cycle.

Design control logic.

Add logic and datapath to provide new bypass, insn, etc.

Determine instruction throughput (IPC).

fr-9

Interrupts, Exceptions, and Traps

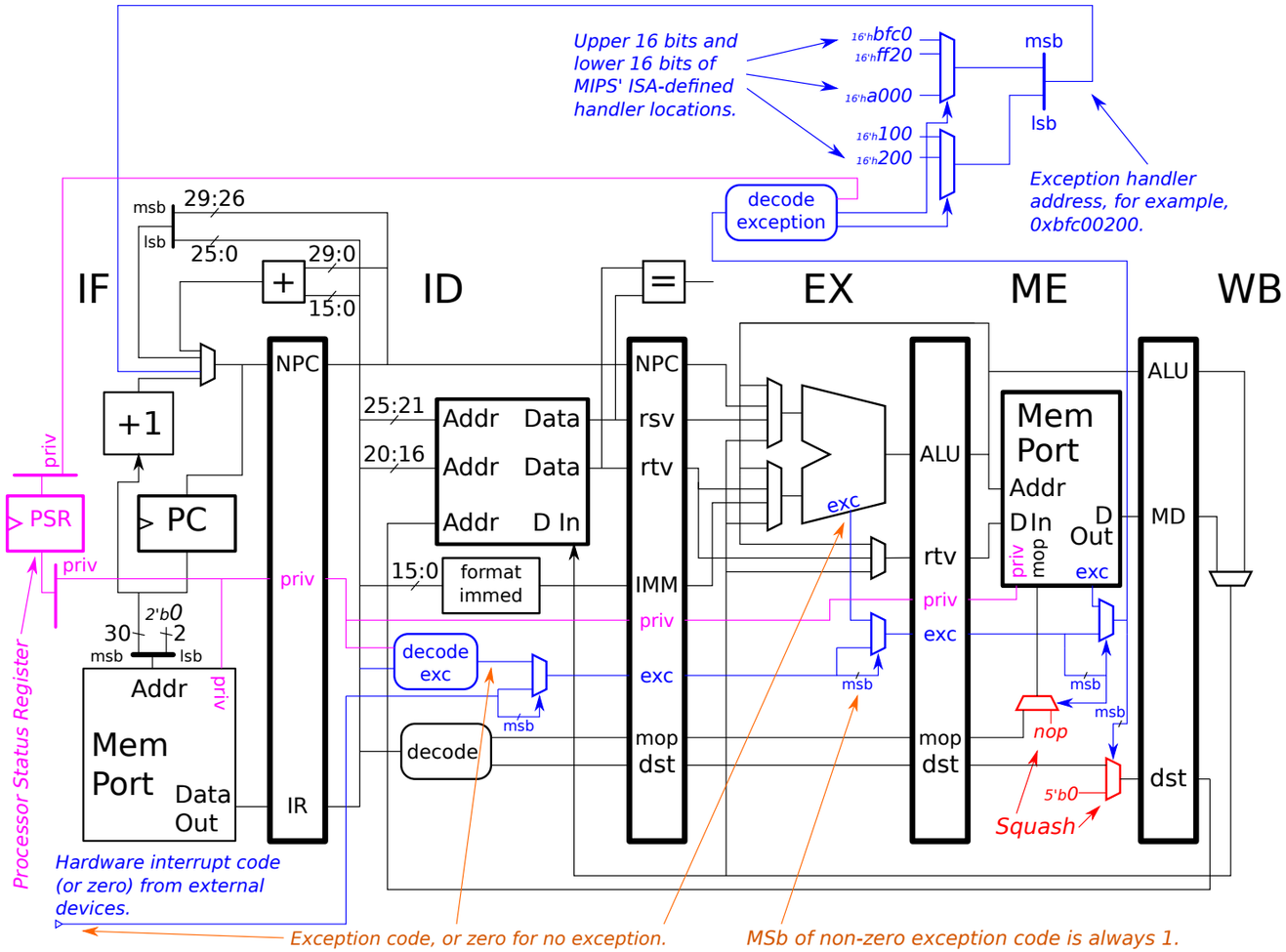
Difference between interrupt, exception, trap.

Causes of exceptions, role of handler.

Privileged Mode.

Pipeline activity leading to execution of handler.

Precise exceptions



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Long Latency (FP) Operations

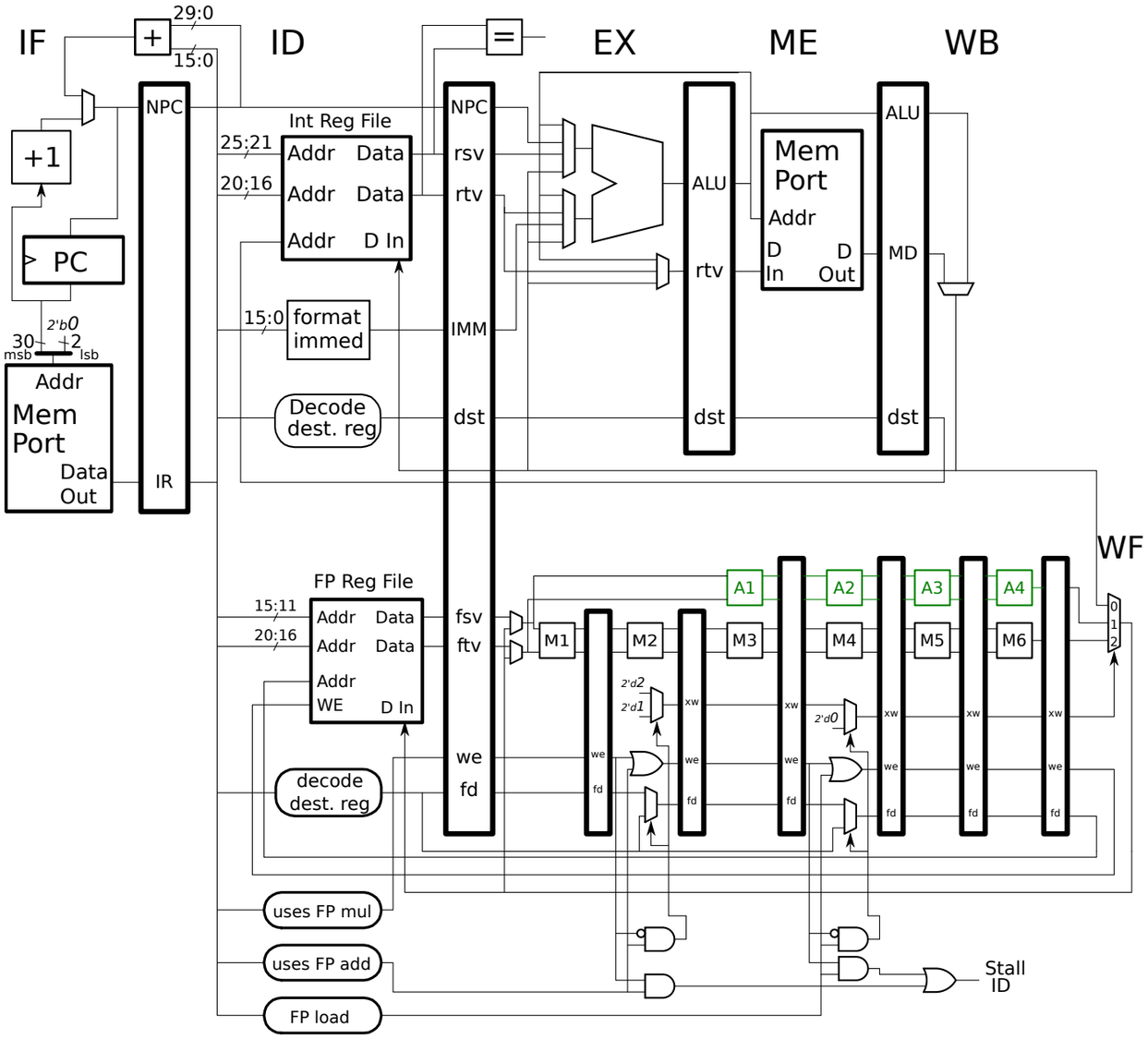
Types of operations. (Floating point and maybe load.)

Degree of pipelining: Initiation interval.

Detecting functional unit structural hazards.

Detecting WB structural hazards: pipeline control logic.

Handling WAW hazards.



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n-Way Superscalar

Duplication of Resources.

Duplicated $n\times$: Fetch, decode, rename, writeback, commit.

Duplicated $< n\times$: load/store, floating-point units.

Costs: $\propto n$ functional units; $\propto n^2$ bypass, control.

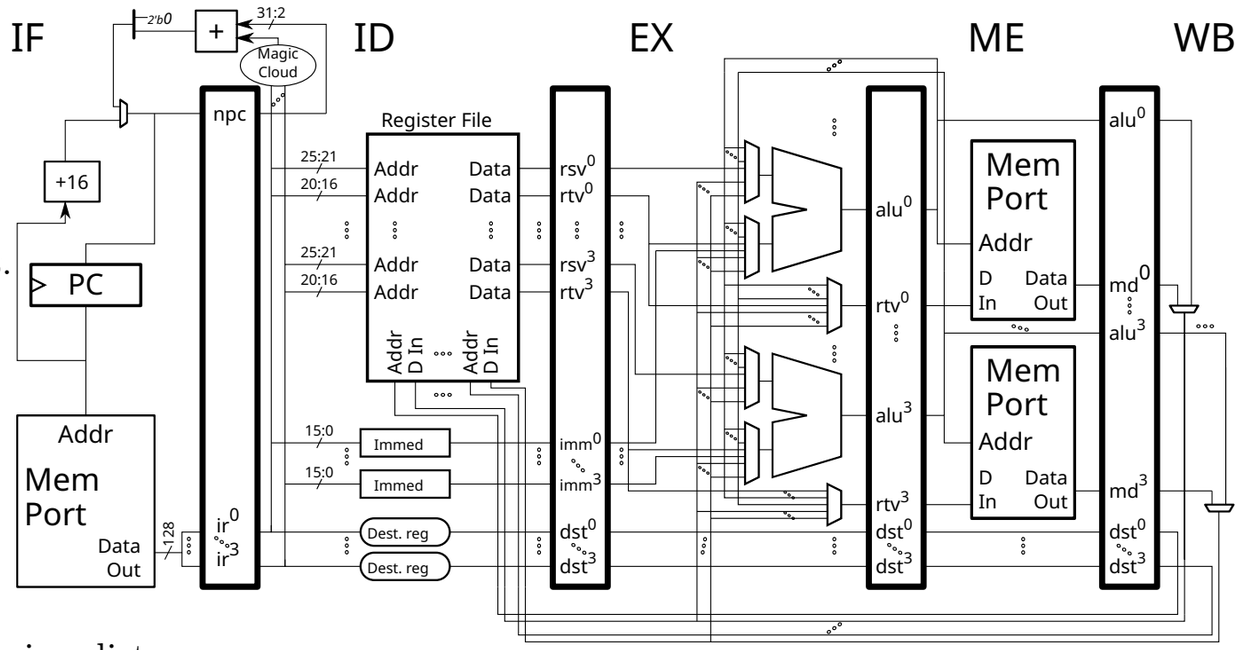
Performance Limiters

Limiters due to device technology: Lower clock with increasing distances.

Aligned groups impose fetch restrictions that reduce fetch efficiency.

More stalls due to data dependencies.

More squashes due to branches.



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VLIW

Difference with superscalar: instruction bundling.

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fr-13

Deeper (Super) Pipelining

Relationship between stage splitting, clock frequency and performance.

Relationship between stage splitting and cost.

- Latch setup time.
- More stalls due to data dependencies.

Vector Instructions

Vector registers.

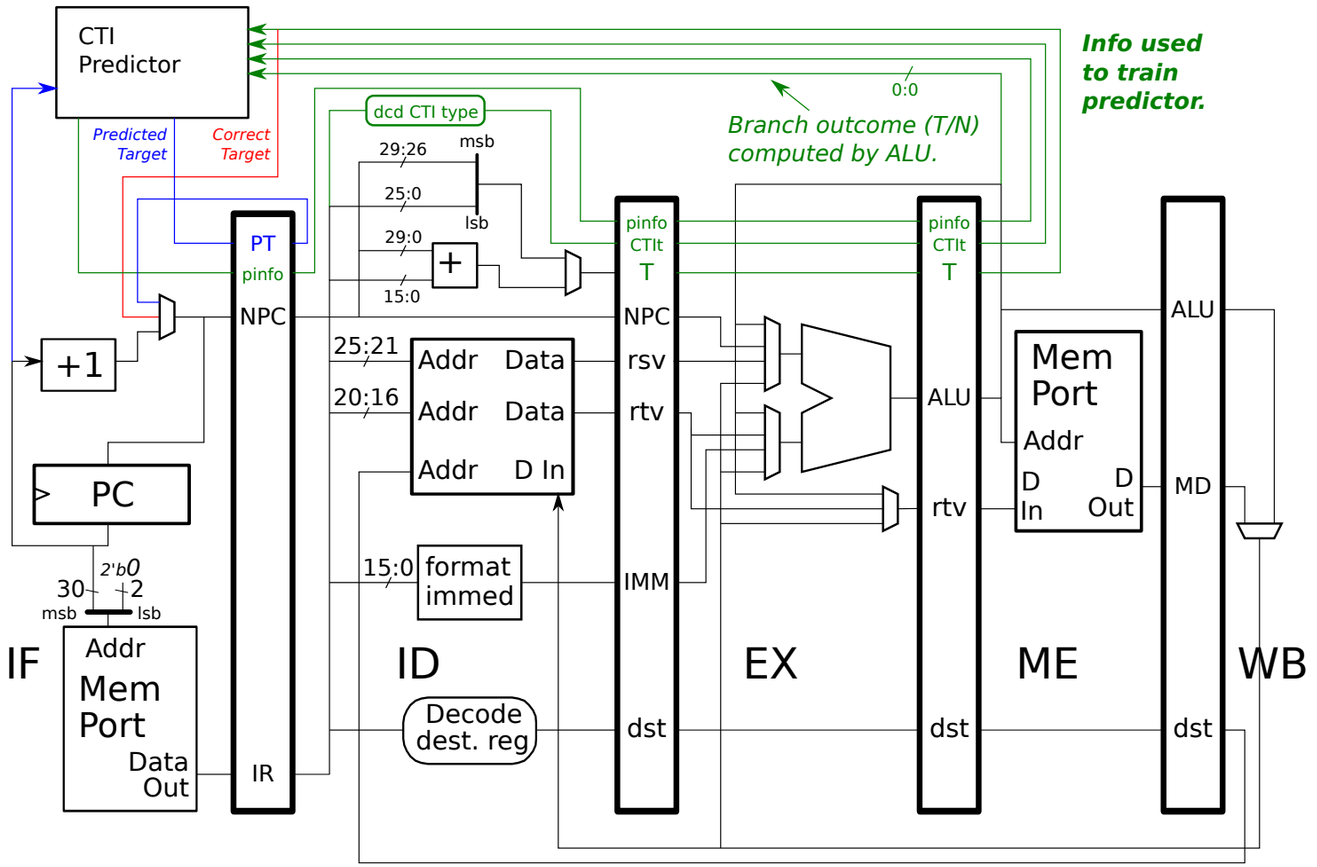
How vector instructions operate on vector registers.

Advantages and disadvantages and differences ...
... between vector instructions and superscalar systems.

CTI Prediction

Definitions, Overview

- Branch Direction Prediction
- CTI Target Prediction
- Where Prediction is Made
- What is Used to Make Prediction
- Misprediction Recovery



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Types of Branch Direction Predictors

Bimodal Predictor.

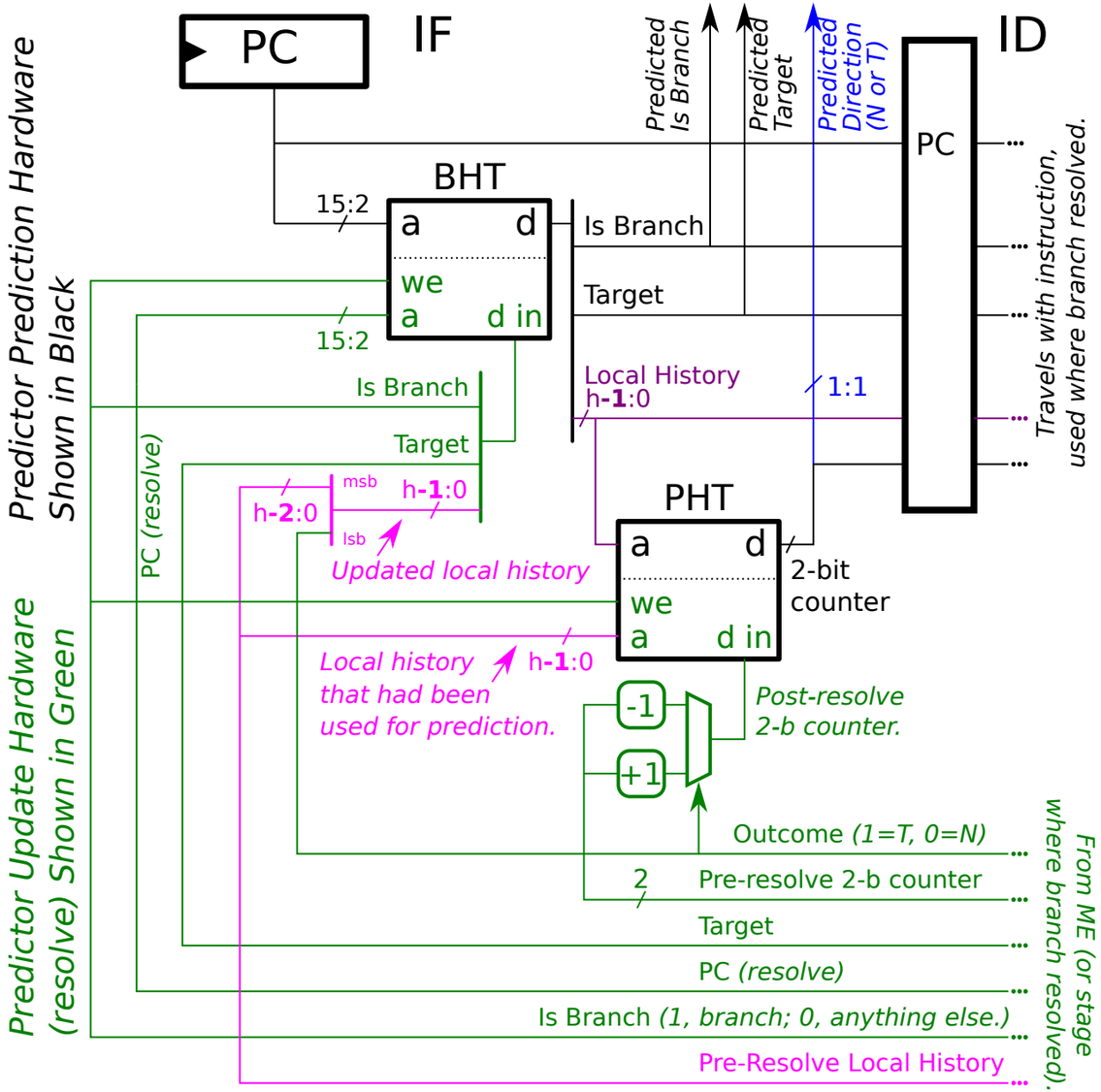
Local History Predictor

Global History Predictor

Global Variations: gshare, gselect.

Less Important Topics

Branch target prediction.



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fr-17

General

Definitions

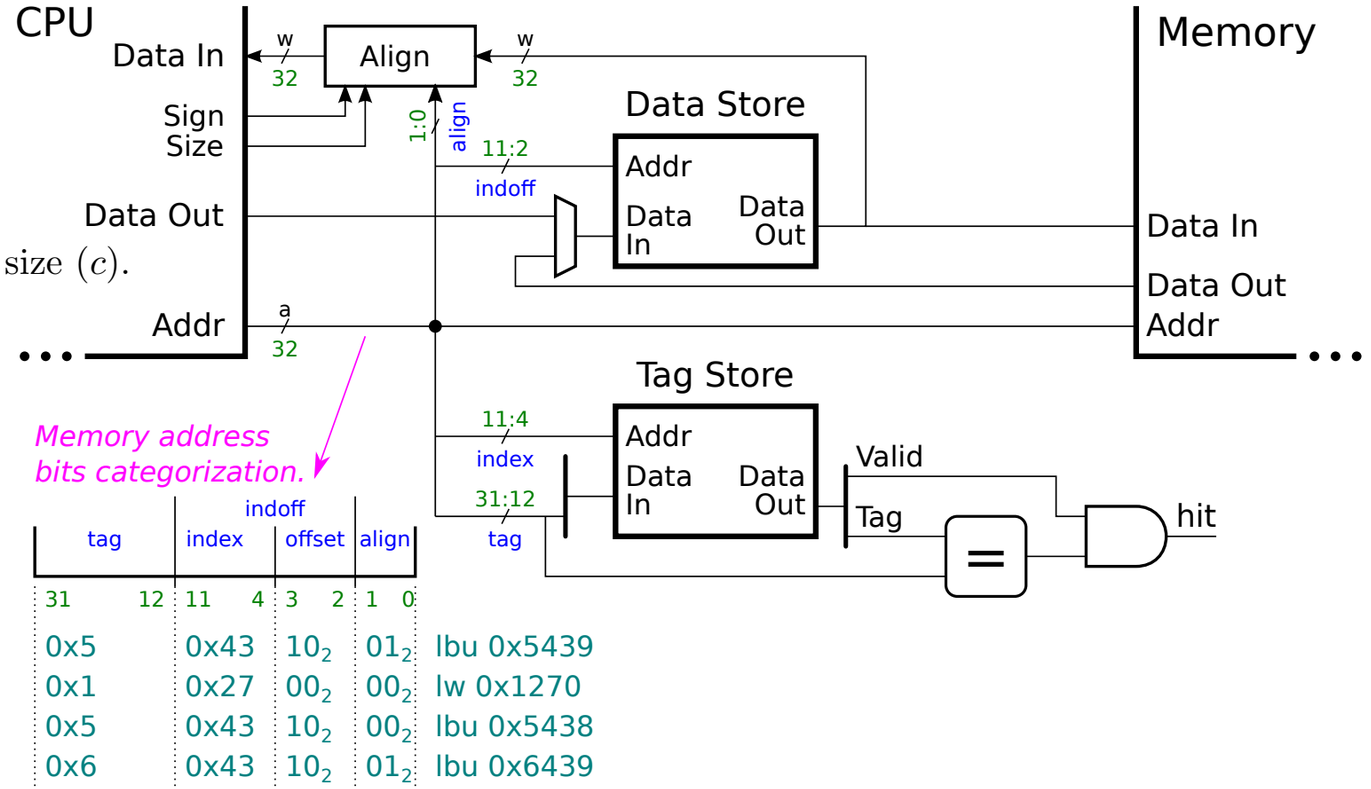
Bus width (w), address space size (a), character size (c).

Caches

Cache structure, connection of memory devices.

Line size implications.

Computing hit ratio for given program.



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fr-18