LSU EE 4720 Homework 3 Due: 28 March 2024

Collaboration Rules

Each student is expected to complete his or her own assignment. It is okay to work with other students and to ask questions in order to get ideas on how to solve the problems or how to overcome some obstacle (be it a question of MIPS or assembler syntax, interpreting error messages, how a part of the problem might be solved, etc.) It is also acceptable to seek out assembly language resources for help on MIPS, etc. It is okay to make use of AI LLM tools such as ChatGPT and Copilot to generate sample code. (Do not assume LLM output is correct. Treat LLM output the same way one might treat legal advice given by a lawyer character in a movie: it may sound impressive, but it can range from sage advice to utter nonsense.)

After availing oneself to these resources **each student is expected to be able to complete the assignment alone**. Test questions will be based on homework questions and **the assumed time needed to complete the question will be for a student who had solved the homework assignment on which it was based**.

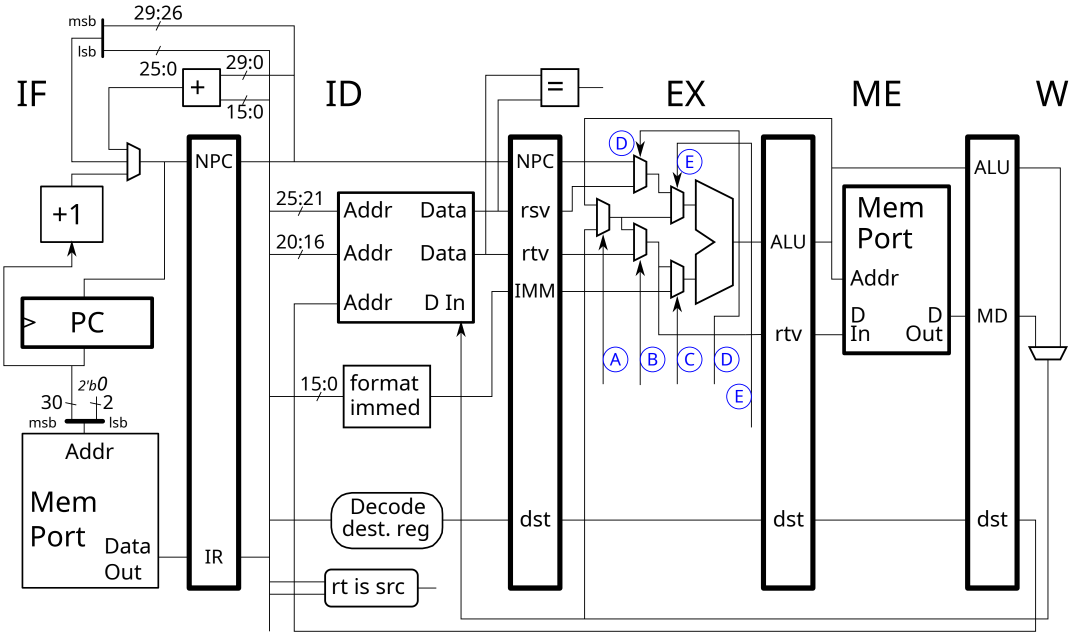
Student Expectations

Some of the problems require thought, and students are expected to persevere until they find a solution. It is the students' responsibility to resolve frustrations and roadblocks quickly, and hopefully with the satisfaction of making progress. There are plenty of old problems and solutions to look at. One way to resolve issues is to ask Dr. Koppelman or others for help.

For the 2020 Final Exam, and other exams and solutions visit `https://www.ece.lsu.edu/ee4720/prev.html`*.*

Problem 1 on the next page.

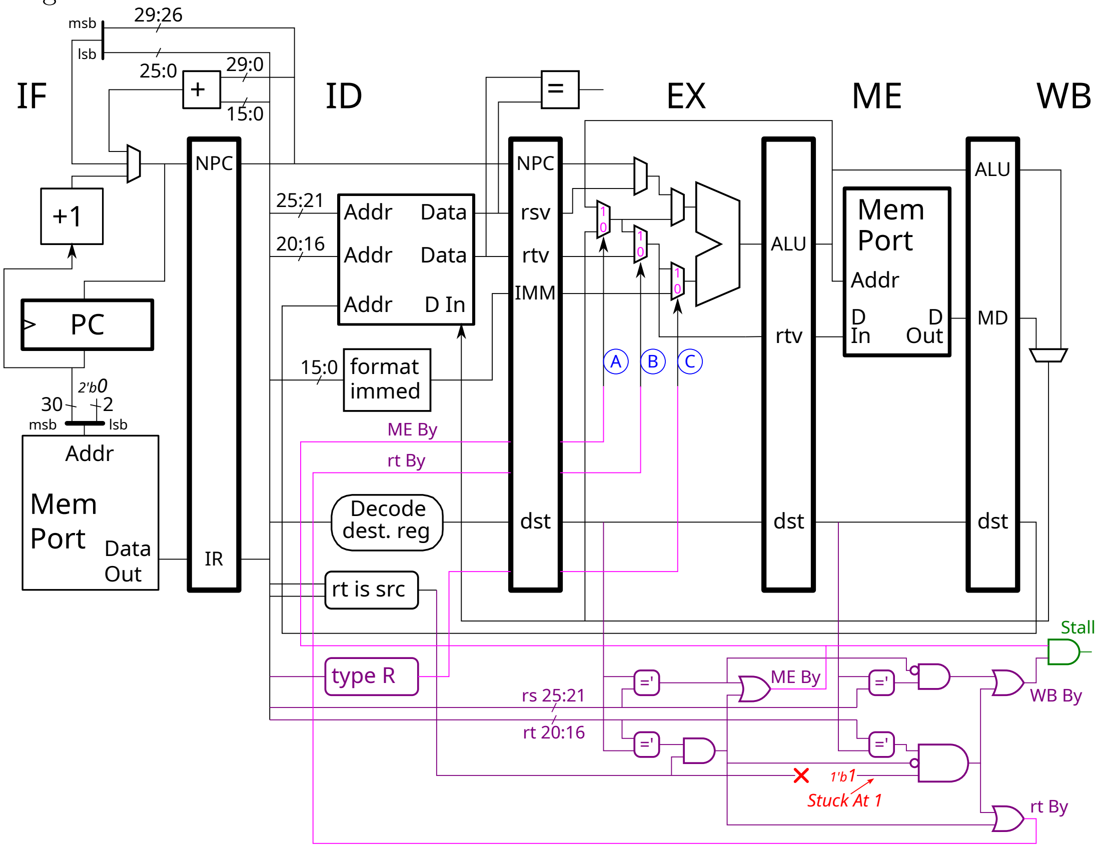
Problem 1: Appearing below is the slightly lower cost MIPS implementation from the 2020 midterm exam. In the 2020 exam three EX-stage select signals were labeled, (A-C), here all five are, (A-E). Below that is an incomplete pipeline execution diagram (it lacks a code fragment) and a timing diagram showing values on the labeled select signals over time. In 2020 midterm exam Problem 1(a) these signal values had to be found given a code fragment. For this problem, the signal values are given. Write a code fragment that could have produced these signals. Feel free to look at the solution to 2020 Problem 1(a) for help and practice.



□ Write a program that could have resulted in these select signal values.

```
# Cycle                     0     1     2     3     4     5     6     7

                            IF    ID    EX    ME    WB

                                  IF    ID    EX    ME    WB

                                        IF    ID    EX    ME    WB

                                              IF    ID    EX    ME    WB

# Cycle                     0     1     2     3     4     5     6     7
A                                       X     0     1     0
B                                       X     1     0     0
C                                       1     0     0     1
# Cycle                     0     1     2     3     4     5     6     7
D                                       1     X     X     1
E                                       0     1     1     0
# Cycle                     0     1     2     3     4     5     6     7
```

Problem 2: Appearing below is the solution to 2020 Midterm Exam Problem 2, showing control logic for those slightly lower cost bypass paths, with one unfortunate change. The bottom input to the 3-input AND gate is supposed to connect to the rt is src logic block. Due to some defect that input is stuck at 1. (This is known as a *stuck-at* fault.) This stuck-at fault is shown on the diagram.



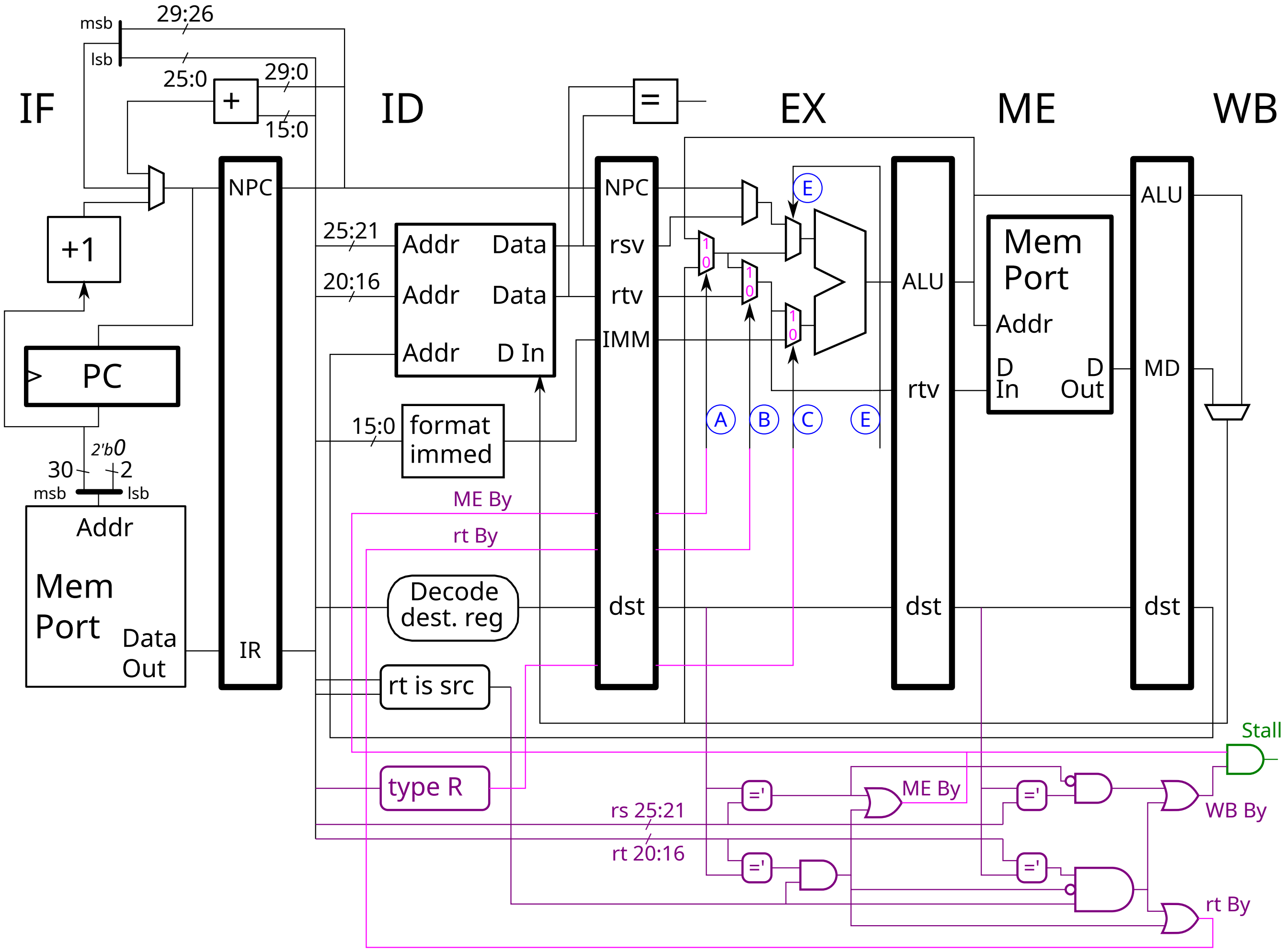
□ Write a code fragment that will not execute as intended on this hardware due to the stuck-at fault. *Note: In the original assignment the phrase "execute correctly" was used instead of "execute as intended".*

As luck would have it this defect has occurred in a computer that's on Mars. The computer can't be fixed, but it is possible to download new software to this computer.

□ Can the software be re-written to avoid this stuck-at fault? □ Explain.

Problem 3: Appearing below is the slightly lower cost MIPS implementation, including the control logic from the 2020 Midterm Exam solution. Design the control logic for the select signal labeled E. *Hint: Not much needs to be added if some existing logic is used.* The SVG source for the diagram can be found at `https://www.ece.lsu.edu/ee4720/2024/hw03-lite-logic-e.svg`.

□ Design control logic for select signal E.



IF
ID
EX
ME
WB
msb
lsb
29:26
25:0
29:0
15:0
+
=
NPC
+1
PC
2'b0
30
2
msb
lsb
Addr
Mem Port
Data Out
IR
25:21
20:16
Addr
Data
Addr
Data
Addr
D In
15:0
format immed
NPC
rsv
rtv
IMM
dst
E
A
B
C
E
1
0
ALU
rtv
dst
Mem Port
Addr
D In
D Out
ALU
MD
dst
ME By
rt By
Decode dest. reg
rt is src
type R
rs 25:21
rt 20:16
=
ME By
WB By
rt By
Stall