**LSU EE 4720** **Homework 6** Solution **Due: 28 April 2023**

**Problem 1:** Solve 2022 Final Exam Problem 2, in which code fragments are either written or analyzed for our MIPS FP implementation.

See the final exam solution at `https://www.ece.lsu.edu/ee4720/2022/fe_sol.pdf`.

**Problem 2:** Solve the last part of 2022 Final Exam Problem 1, the one with the 4-way superscalar pipeline. (You can tell it's 4-way because the superscripts range from 0 to 3.) There is no need to show superscripts on the stage labels in your execution diagram. For sample problems see past final exams, such as 2021 Problem 2.

See the final exam solution at `https://www.ece.lsu.edu/ee4720/2022/fe_sol.pdf`.

*There is another problem on the next page.*

**Problem 3:** Appearing below is our MIPS FP implementation but with an unpipelined FP add unit. Some of the control logic needed to generate stalls when a FP add instruction is in flight is in the magic cloud labeled "Future HW Solution". Design that logic. For similar logic see the logic on the Partially Pipelined pages from Set 9 slides (about page 14). *Hint: This does not require much hardware.* For similar problems see 2020 Spring Homework 5 and 2020 Spring Final Exam Problem 2.

Use the execution below to help you design the hardware:

```
# Cycle          0  1  2  3  4  5  6  7  8  9  10 11 12 13 14
add.d f0, f2, f4 IF ID A  A  A  A  WF
add.d f6, f8, f10   IF ID -------> A  A  A  A  WF
addi r1, r1, 8         IF -------> ID EX ME WB
add.d f12, f18, f14                IF ID ----> A  A  A  A  WF
# Cycle          0  1  2  3  4  5  6  7  8  9  10 11 12 13 14
```

An SVG version of the image can be found at `https://www.ece.lsu.edu/ee4720/2023/hw06-fp-aaaa.svg`, use Inkscape or some other SVG editor, or even a text editor.

The solution appears below in blue. The OR gate now has three new inputs, which are the `ad` signals in the `M3`, `M4`, and `M5` stages.