LSU EE 4720 **Homework 5** Solution **Due: 27 April 2020**

It's up to all of us: $r > 2\,\mathrm{m} \;\Rightarrow\; R_e < 1$ where r is the radius of the largest circle with you at the center and containing only people in your household, and R_e is the *effective reproduction number*, the number of people infected by an infectious person.

Problem 1: **Solve 2019 Final Exam Problem 2**, which asks for a pipeline execution diagram of FP code on our FP MIPS implementation, but with the comparison functional unit and floating-point condition code register added. For more information on the implementation of the floating-point compare instructions see 2018 Final Exam Problem 3. Please don't get confused about which problem to solve and which to use for background!

See the posted final exam solution.

Problem 2: The following question appeared as Spring 2010 Homework 3 Problem 3, but in this ten-year anniversary version the solution must contain control logic for the multiplexors at the inputs to the `A1` and `A2` units. Try to initially solve it without looking at the solution, but use the solution if you get stuck.

Replace the fully pipelined adder in our FP pipeline (which appears on the next page) with one with an initiation interval of two and an operation latency of four. (The existing FP adder has an initiation interval of one and an operation latency of four.) See 2010 Homework 3 Problem 3 for more details.

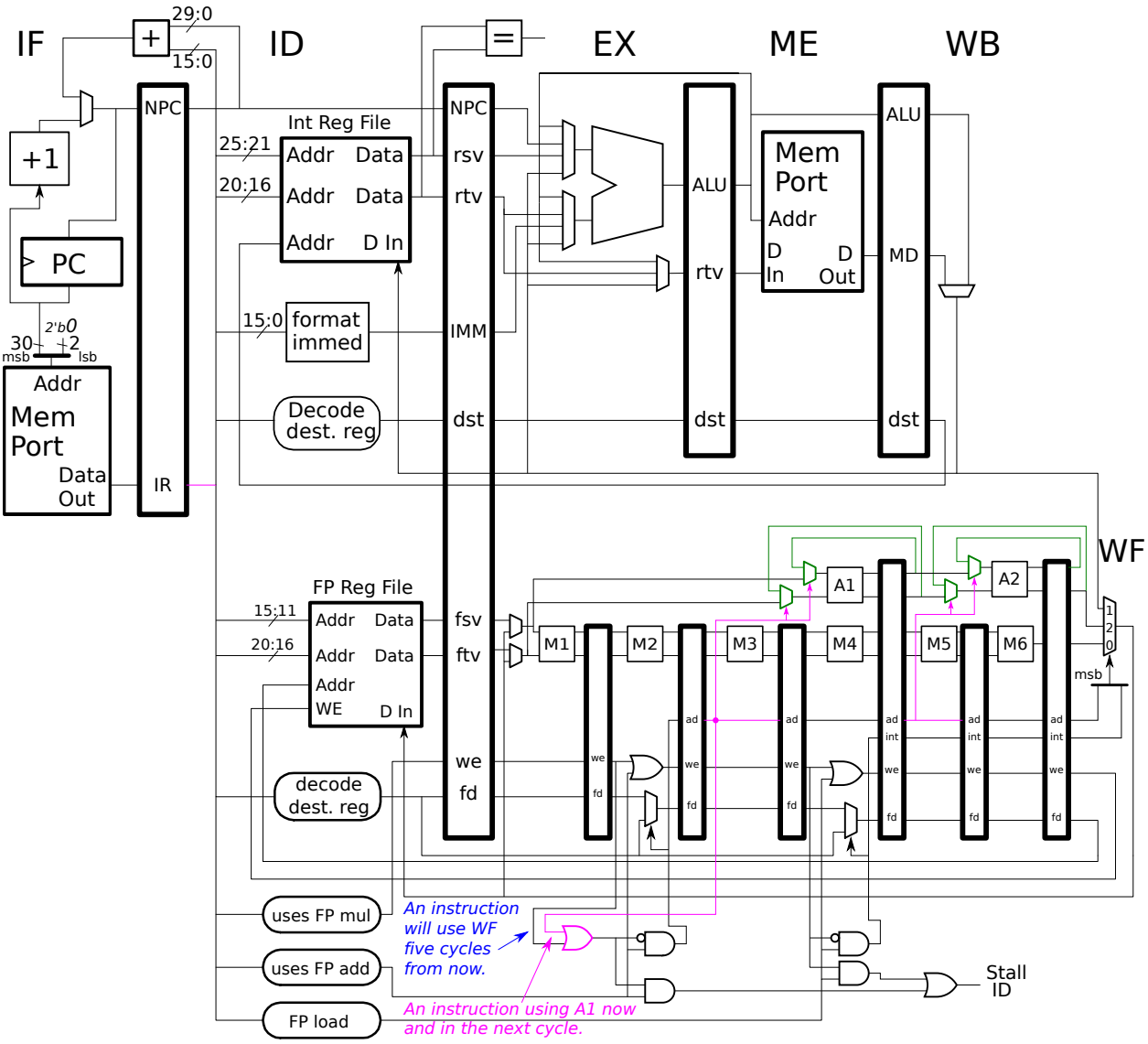
Show datapath and control logic. Be sure to show control logic for the multiplexors at the inputs to `A1` and `A2`, **this control logic does not appear in the solution to the 2010 assignment**. *Hint: This additional control logic is really easy to do, it can be done just with wires, no gates!*

Solution on next page.

Solution appears below. Note to Spring 2020 students: The control logic for the WF-stage mux is different, perhaps simpler, than in the FP pipelines used elsewhere in class. The `ad` pipeline latch signal is 1 in stages with an instruction using the FP add functional unit. The connections to the `ad` pipeline latch are equivalent to connections to the LSB (bit `0:0`) of the `xw` pipeline latch. *Note to future students: the* `WF`*-stage mux logic here might be used in the default class FP pipeline in future semester.*

The changes in green allow data to pass through the `A1` and `A2` units twice. The control logic, in purple provides the select signal for the new multiplexors at the `A1` and `A2` inputs.

The stall condition for an `add.s` in `ID` must now check for an `add.s` in the first pass through `A1`, those two conditions are checked by the purple OR gate.



An Inkscape SVG version of the MIPS implementation below can be found at
`https://www.ece.lsu.edu/ee4720/2020/mpipei_fp_by.svg`.