LSU EE 4720

Attention Perfectionists: An Inkscape SVG version of the illustration of the superscalar MIPS implementation used in the final exam problems and their solution for this assignment can be found at http://www.ece.lsu.edu/ee4720/2016/fe-ss.svg and http://www.ece.lsu.edu/ee4720/2016/fe-plabc-sol.svg.

Problem 1: Answer Spring 2016 Final Exam Problem 1 a, b, and c, in which a single memory port is connected to the ME stage of a two-way superscalar MIPS implementation. The solution to this problem is available. Make a decent attempt to solve this problem on your own, without looking at the solution. Only peek at the solution for hints and use the solution to check your work. See posted final exam solution at http://www.ece.lsu.edu/ee4720/2016/fe_sol.pdf.

Problem 2: Answer Spring 2016 "Final Exam Problem" 1e, which asks for modifications to a 2-way supescalar MIPS implementation that avoids stalls for certain pairs of load instructions. *Note: Problem 1d was given on the final exam. Problem 1e, which did not appear on the final, is an expanded version of Problem 1d.*

See posted final exam solution at http://www.ece.lsu.edu/ee4720/2016/fe_sol.pdf.