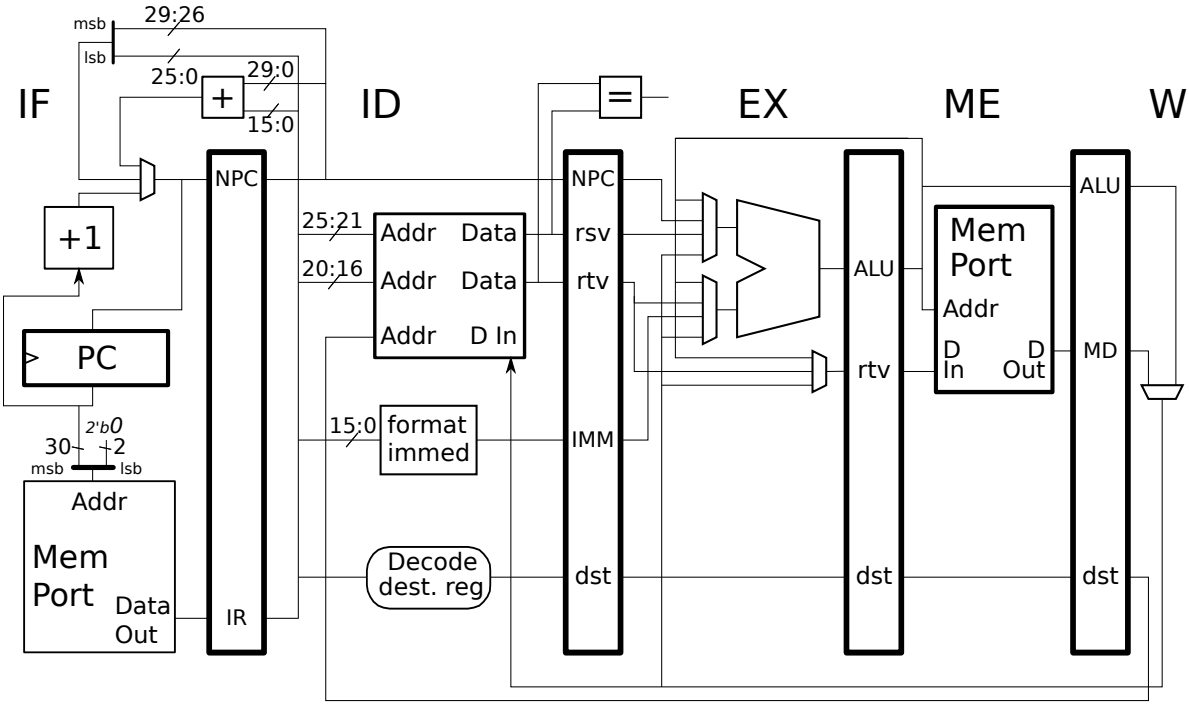
LSU EE 4720 **Homework 2** **Due: 17 February 2017**

Problem 1: The following problems are from the 2016 EE 4720 Final Exam.

(*a*) *The following problem appeared as 2016 EE 4720 Final Exam Problem 2a. (Just 2a, not 2b).* Show the execution of each of the two code fragments below on the illustrated MIPS implementations. All branches are taken. Don't forget to check for dependencies.

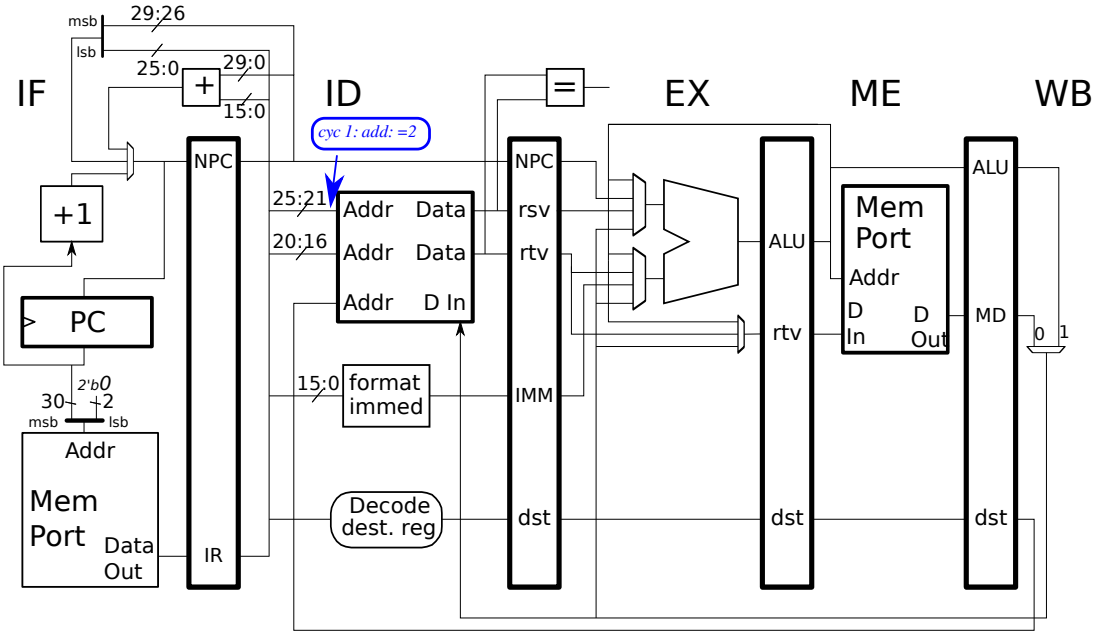



```
# CODE SEQUENCE A
add r1, r2, r3

sub r4, r1, r5
```

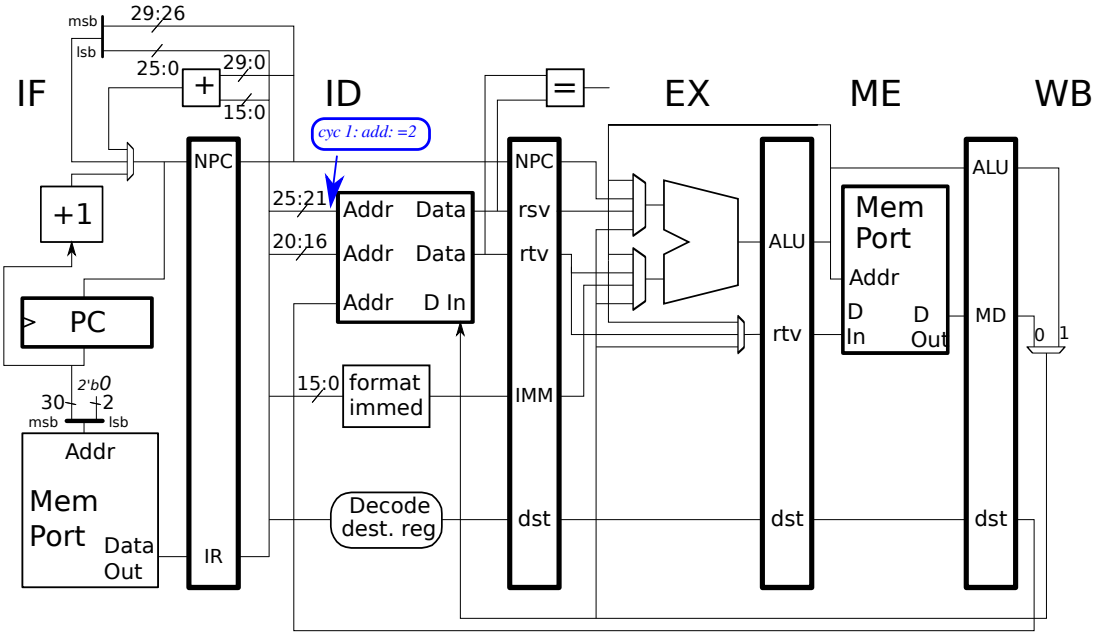
Show execution of the following code sequence.

```
# CODE SEQUENCE B
beq r1, r1 TARG

or  r2, r3, r4

sub r5, r6, r7

xor r8, r9, r10

TARG:
lw r10, 0(r11)
```

(*b*) For each of the two code sequences above label each used wire on the diagram below with: the cycle number, the instruction, and if appropriate a register number or immediate value. For example, the register file input connected to `ID.IR` bits 25:21 should be labeled 1: add, =2 because in cycle 1 the `add` instruction is using that register file input to retrieve register `r2`. See the illustration below. **Only** label wires that are **used** in the execution of an instruction. For example, there should not be a label 2: sub, =1 because the value of `r1` will be bypassed. Instead, label the bypass path that is used. Pay particular attention to wires carrying branch information and to bypass paths. Look through old homeworks and exams to find similar problems.
For Code Sequence A:



For Code Sequence B:



Problem 2: *The following problem is from 2016 EE 4720 Final Exam Problem 5a.* Suppose that a new ISAis being designed. Rather than requiring implementations to include control logic to detect dependencies the ISA will require that dependent instructions be separated by at least six instructions. As a result, less hardware will be used in the first implementation.

(*a*) Explain why this is considered the wrong approach for most ISAs.

(*b*) What is the disadvantage of imposing this separation requirement?