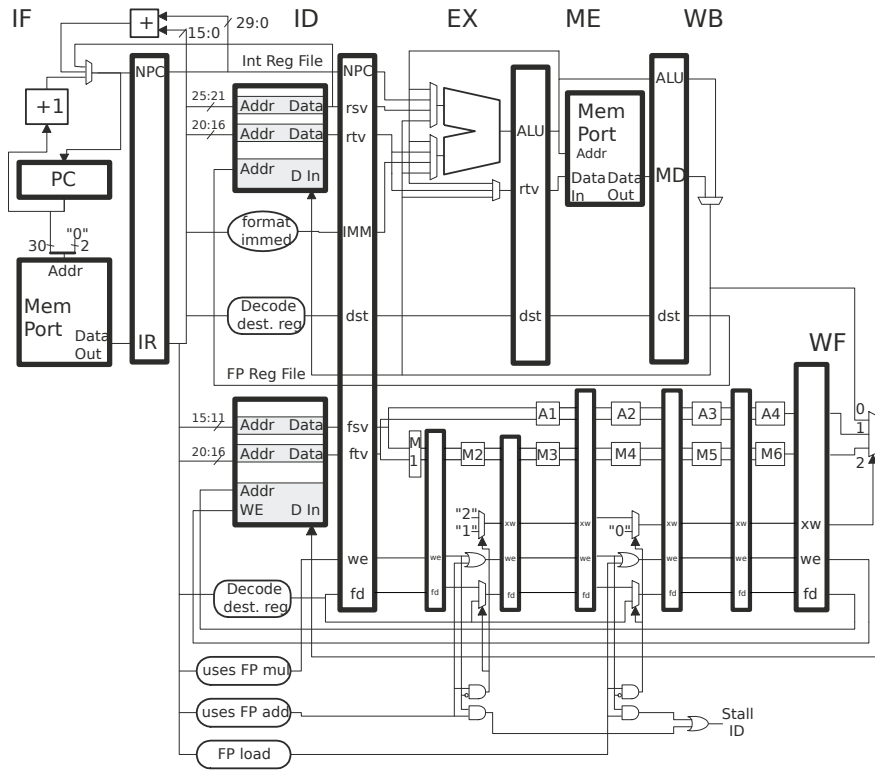


Problem 1: The following code fragments execute incorrectly on the following pipeline. For each fragment describe the problem and correct the problem.



(a) Describe problem and fix problem.

```
lwc1 f2, 0(r1)    IF ID EX ME WF
add.s f1, f2, f3  IF ID A1 A2 A3 A4 WF
```

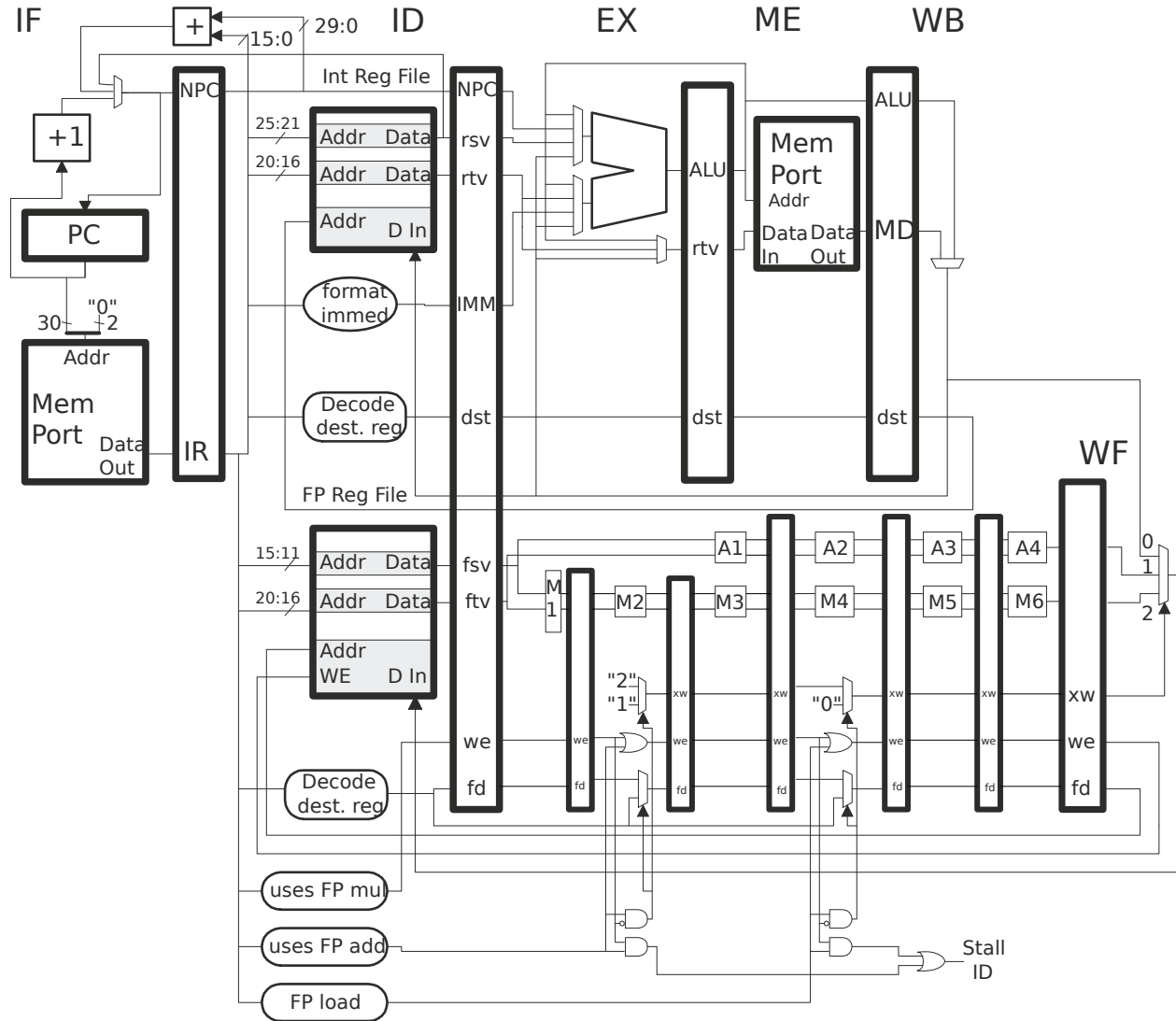
(b) Describe problem and fix problem.

```
add.s f1, f2, f3  IF ID A1 A2 A3 A4 WF
addi r1, r1, 4    IF ID EX ME WB
lwc1 f2, 0(r1)    IF ID EX ME WF
```

(c) Describe problem and fix problem.

```
add.d f1, f2, f3  IF ID A1 A2 A3 A4 WF
```

Problem 2: The code fragment below contains a MIPS floating-point comparison instruction and branch. The pipeline illustrated below does not have a comparison unit, in this problem we will add one. The comparison unit to be used has two stages, named C1 and C2. The output of C2 is one bit, indicating if the comparison was true.



```

c.gt.d f2, f4
bc1t TARG
add.d f2, f2, f10
...
TARG: xor r1, r2, r3

```

(a) Add the comparison unit to the pipeline above. Also add a new register FCC (floating point condition code) that is written by the comparison instruction and is used by the control logic to determine if a floating-point branch is taken.

The FCC register should have a data and write-enable input, show the control logic generating the write-enable signal. Show a cloud labeled “branch control logic” and connect it to appropriate datapath components.

(b) Show the execution of the code sample above on your modified hardware, but without any bypass paths for the added hardware.

(c) Add whatever bypass paths are needed so that the code executes with as few stalls as possible **but** without having a major impact on clock frequency. Assume that C2 produces a result in about 80% of the clock period.

Source files for the diagram are at:

<http://www.ece.lsu.edu/ee4720/2014/mpipeifp.eps>,

<http://www.ece.lsu.edu/ee4720/2014/mpipeifp.svg>. The svg file can be edited using Inkscape. ■