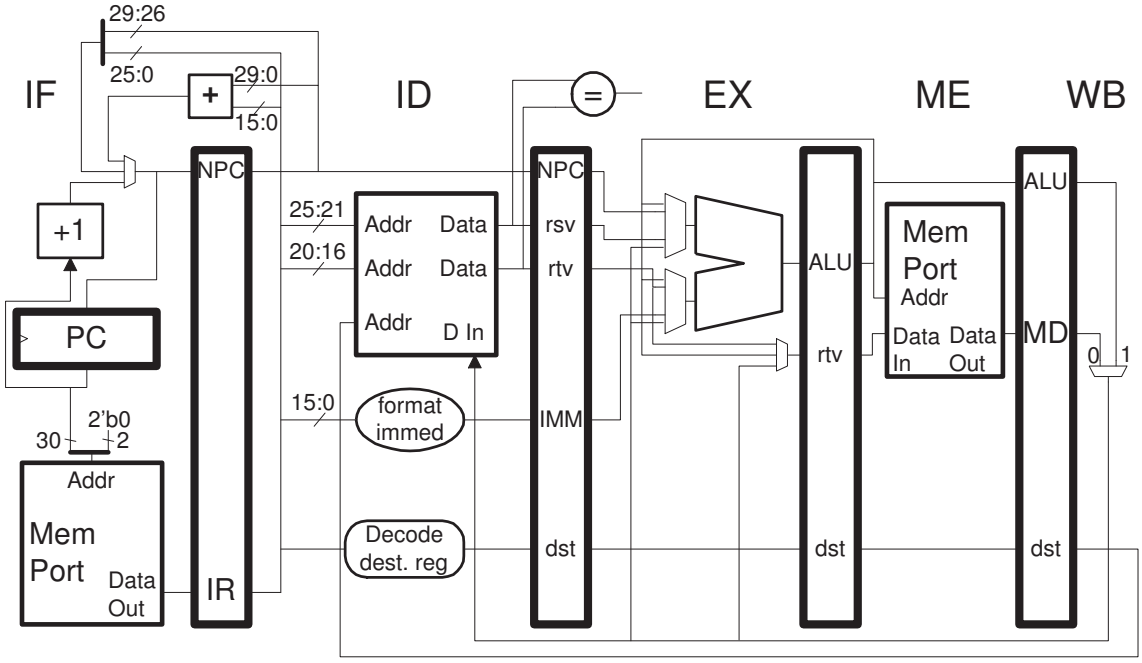
LSU EE 4720 **Homework 3** **Due: 22 September 2010**

Problem 1: *Note: Problems like this one have been assigned before. Please solve this problem without looking for a solution elsewhere. If you get stuck ask for hints. Copying a solution will leave you unprepared for exams, and will waste your (or your parents') hard-earned tuition dollars.* A shift unit is to be added to the EX stage of the implementation below. The shift unit has a 32-bit data input, `VIN`, a 5-bit shift amount input, `AMT`, a 1-bit input `SIN`, and a 1-bit control input `DIR`. There is a 32-bit data output, `VOUT`. The `DIR` input determines whether the shift is left (1) or right (0). If the shift is right then the value at input `SIN` is shifted in to the vacated bit positions. The meaning of the other inputs is self-explanatory. For a description of MIPS-I instructions see the MIPS32 Volume 2 linked to the course references page.



(*a*) Connect the shift unit data inputs so that it can be used for the MIPS `sll`, `sllv`, `srl`, `srlv`, `sra`, and `srav` instructions. Assume that the ALU has plenty of slack (it is not close to carrying the critical path). (Control inputs are in the next part.)

- Be sure your design does not unnecessarily inflate cost or lower performance.
- In your diagrams be sure to use the bit ranges used, for example, 27:21, when connecting a wire to an input with fewer bits than the wire.

(*b*) Show the logic for control inputs `DIR` and `SIN` and any multiplexors that you added.

(*c*) Repeat the design of the datapath but assuming that the ALU is on the critical path and that we don't want to lower the clock frequency.