LSU EE 4720 **Homework 4** **Due: 3 December 2007**

Problem 1: *For answers to this problems consult the SPARC Architecture Manual Version V8, linked to the course references page.*

Suppose a SPARC V8 trap table has been set up at address `0x12340000`.

(*a*) Write a SPARC V8 program that sets the trap base register (TBR) to that address. Assume the processor is already in privileged mode. *Hint: A correct solution consists of two instructions, a three-instruction program is okay too.*

Call the SPARC V8 instruction that writes the TBR *foo*. The ISA definition of `foo` makes it easy to design the control logic and bypassing hardware on **certain** implementations.

(*b*) What about the definition of foo makes the control logic and bypassing hardware design easy on those certain implementations?

(*c*) Why not do the same for, say, the `add` instruction?

(*d*) Describe an implementation in which the control logic for `foo` would not be so simple despite the "help" from the ISA definition.

Problem 2: Solve the EE 4720 Spring 2007 Final Exam problem 1.

Problem 3: Solve the EE 4720 Spring 2007 Final Exam problem 3.