LSU EE 4720 **Homework 3** **Due: 18 April 2007**

Some of the questions below are about the interrupt mechanisms defined for the MIPS32, SPARC V8, and PowerPC 2 ISAs. MIPS and SPARC interrupt mechanisms were covered in class, PowerPC's mechanism was not. All are documented in manuals linked to the class references page, `http://www.ece.lsu.edu/ee4720/reference.html`. *When using these references keep in mind that interrupt terminology differs from ISA to ISA and that you are not expected to understand (at least on first reading) most of what is in these manuals. Finding the right manuals and the relevant pages in those manuals is part of this assignment's learning experience.*

Problem 1: Consider a load instruction that raises an exception due to a fixable problem with a memory address (for example, a TLB miss, whatever that is) on an implementation of MIP32, SPARC V8, and PowerPC 2.

(*a*) Where does each ISA say the address of the faulting instruction (the load) should be put? Give the exact register name, number, or both (if available).

(*b*) Where does each ISA say to put the memory address that the load attempted to load from?

Problem 2: Is PowerPC's equivalent of a trap table more similar to SPARC's trap table or to MIPS'? Explain and describe how specific elements are the same or different. Look at table placement, size, number of entries, and perhaps other characteristics.

Problem 3: In class a precise exception was defined as one in which, to the handler it appears that all instructions before the faulting instruction have completed normally and that the faulting instruction and those following it have not executed (correctly or otherwise). PowerPC calls certain exceptions precise even though they violate this rule. What are they and how is this violation justified in the manual?

Problem 4: Solve Fall 2006 Final Exam Problem 1. *Note: At the time this was assigned the solutions were not available.*