

Name _____

Computer Architecture
EE 4720
Midterm Examination
Friday, 27 October 2006, 12:40–13:30 CDT

Problem 1 _____ (50 pts)

Problem 2 _____ (20 pts)

Problem 3 _____ (30 pts)

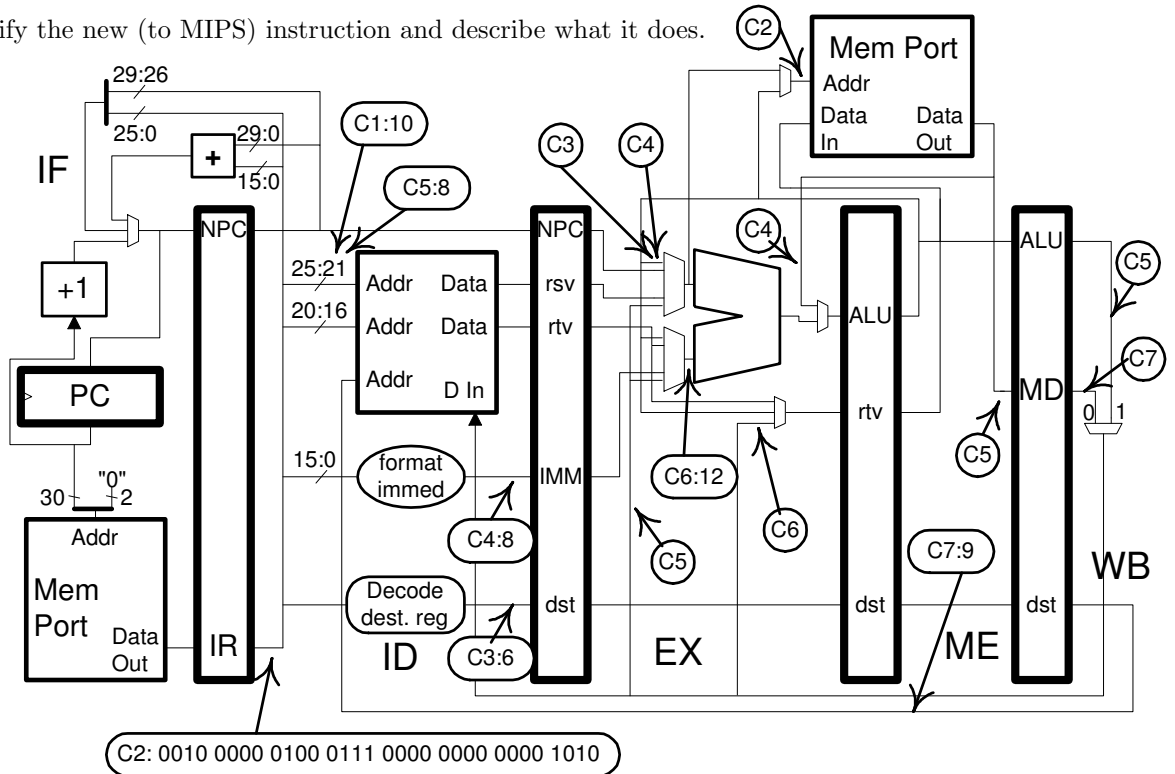
Alias _____

Exam Total _____ (100 pts)

Good Luck!

Problem 1: In the MIPS implementation below the data memory port is in an unusual position that *avoids a stall* and allows the implementation of a *new (to MIPS but not CISC ISAs) instruction*. Some wires are labeled with cycle numbers and values that will then be present. For example, **C1:10** indicates that at cycle 1 the wire will hold a 10. Other wires are labeled just with cycle numbers, indicating that the wire is used at that cycle. If a value on any labeled wire is changed the code would execute incorrectly. [50 pts]

- Write a program consistent with these labels.
- All register numbers and immediate values can be determined.
- Identify the new (to MIPS) instruction and describe what it does.



Cycle: 0 1 2 3 4 5 6 7 8

	IF	ID	EX	ME	WB				

Cycle: 0 1 2 3 4 5 6 7 8

Problem 2: Answer each question below.

(a) Both the SPARC `subcc` and MIPS `slt` instructions below determine if the contents of `r1` (`g1`) is less than `r2` (`g2`).

```
! SPARC
subcc g1, g2, g3
```

```
# MIPS
slt r3, r1, r2
```

[5 pts] Show where each writes the comparison result, what is written, and how the result is used for a branch.

[5 pts] Describe two ways in which the SPARC instruction is more powerful.

(b) One advantage of variable-length ISAs is that programs are shorter (take up less memory). For each code fragment below show how CISC instructions can reduce code size using the MIPS code below as the starting point of an example: Make up CISC instruction(s) for the code below, show how they might be encoded, and indicate how much smaller the code fragments are with the CISC instructions.

[5 pts] New CISC instruction(s). Encoding. Size Reduction.

```
lui r1, 0x1234
ori r1, r1, 0x5678
add r2, r2, r1
```

[5 pts] New CISC instruction(s). Encoding. Size Reduction.

```
jr r31
```

Problem 3: Answer each question below.

(a) The SPECcpu2006 benchmark contains two suites, CINT2006 and CFP2006.

[8 pts] Why are there two suites? What would be the disadvantage of combining them into one suite?

(b) A company develops a new ISA and some implementations of it. It sells the implementations, but keeps the ISA secret.

[8 pts] What's wrong with that?

(c) Operations on packed operand data types often use saturating arithmetic.

[7 pts] What is it and why is it used? Explain using a typical application for packed-operand instructions.

(d) One reason to not use optimization is to make debugging (using a debugger) easier.

[7 pts] Describe two ways optimization makes debugging more difficult. *Hint: Consider single-stepping through code and printing variable values.*