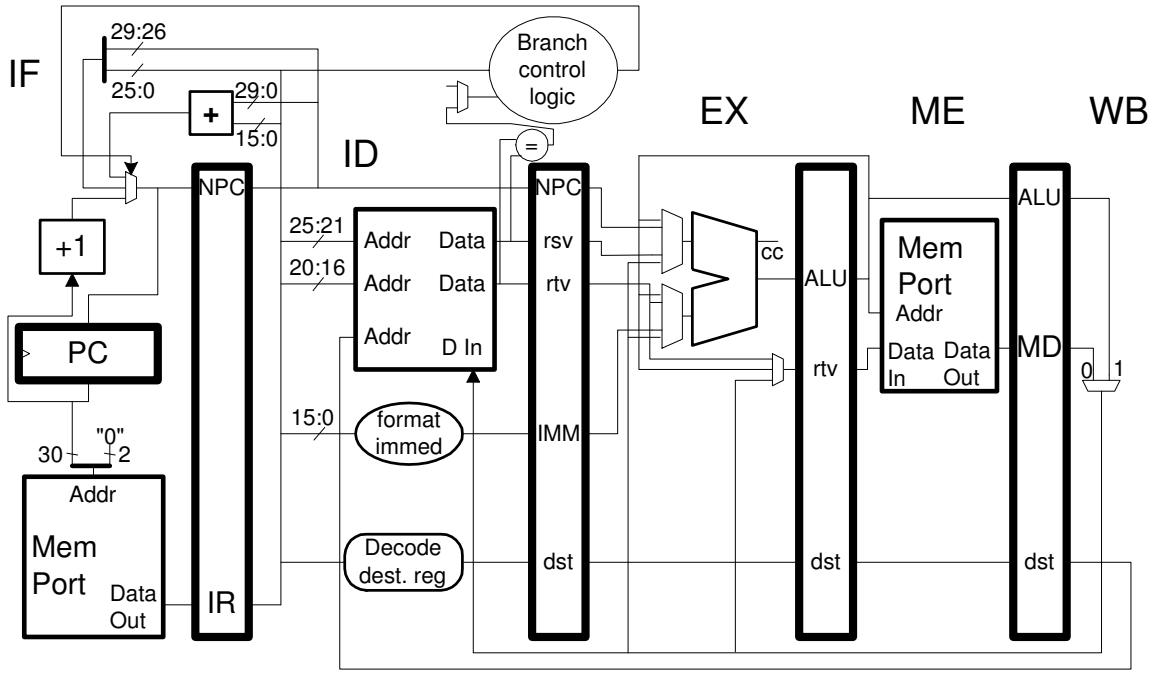
LSU EE 4720 **Homework 3** **Due: 20 October 2006**

Problem 1: Show the changes to the MIPS implementation below needed to implement the SPARC V8 instructions shown in the sub-problems. (See the SPARC Architecture Manual linked to the course references page for a description of SPARC instructions.) Do not show control logic changes or additions. For this problem assume that SPARC has 32 general-purpose registers, just like MIPS. (In reality there are $16n$, $n \geq 4$ general-purpose registers organized into windows. An integer instruction sees only 32 of these but using `save` and `restore` instructions a program can replace the values of 16 of them, the feature is intended for procedure calls and returns. To satisfy curiosity, see the description of register windows in the ISA manual.)



For solution can use larger version on next page.

(*a*) Show the changes for the following instructions. The only changes needed for these are to bit ranges in the ID stage.

```
add %g1, %g2, %g3
sub %g4, 5, %g6
```

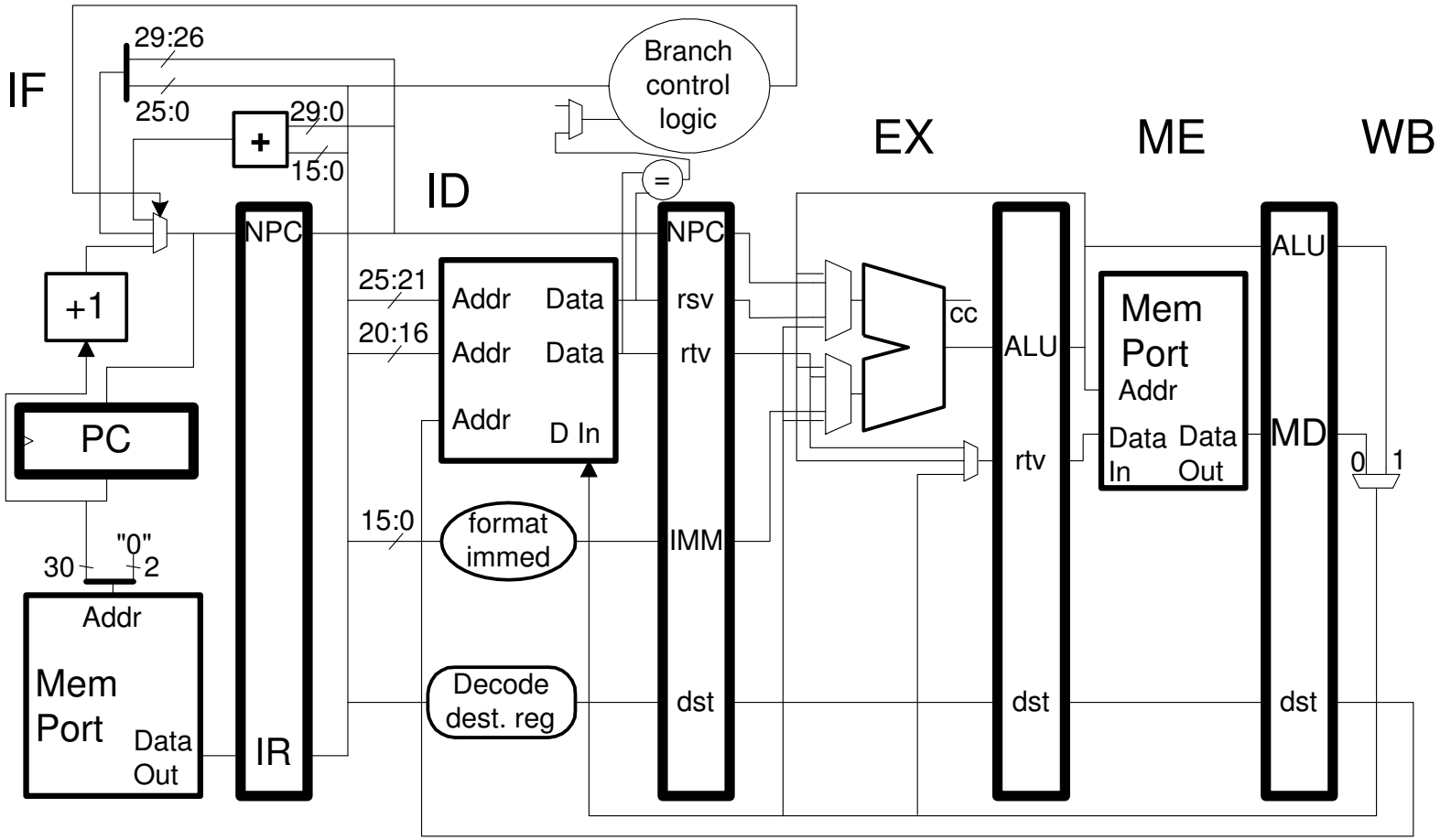
(*b*) Show the changes needed for the store instruction below. This will require more than changing bit ranges.

```
st %g3, [%g1+%g2]
```

(*c*) Show the changes needed to implement the instructions below. The alert student will have noticed the ALU has a new output labeled `cc`. That output has condition code values taken from the result of the ALU operation.

- Don't forget the changes needed for the branch target.
- The changes should work correctly whether or not the branch immediately follows the CC instruction.
- Cross out the comparison unit if it's no longer needed.

```
subcc %g1, %g2, %g3
bge TARG
```


IF
ID
EX
ME
WB
29:26
25:0
29:0
15:0
+
Branch
control
logic
=
NPC
+1
PC
30
"0"
2
Addr
Mem
Port
Data
Out
IR
25:21
20:16
Addr
Data
Addr
Data
Addr
D In
15:0
format
immed
Decode
dest. reg
NPC
rsv
rtv
IMM
dst
cc
ALU
rtv
dst
Mem
Port
Addr
Data
In
Data
Out
ALU
MD
dst
0
1