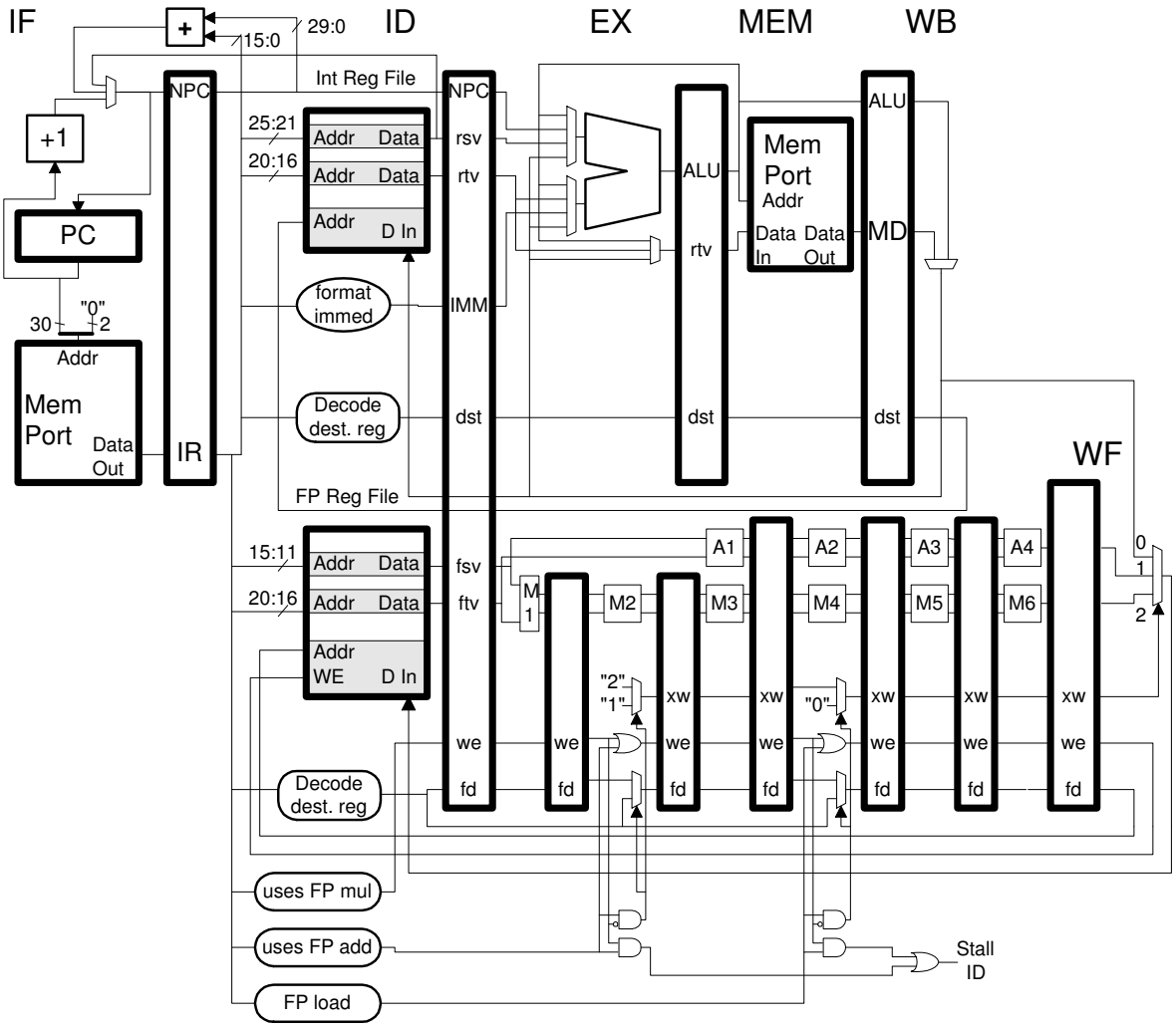
LSU EE 4720 **Homework 4** **Due: 17 April 2006**

Problem 1: The code below executes on the illustrated MIPS implementation. The FP pipeline is fully bypassed but the bypass connections are not shown.



(*a*) Show a pipeline execution diagram.

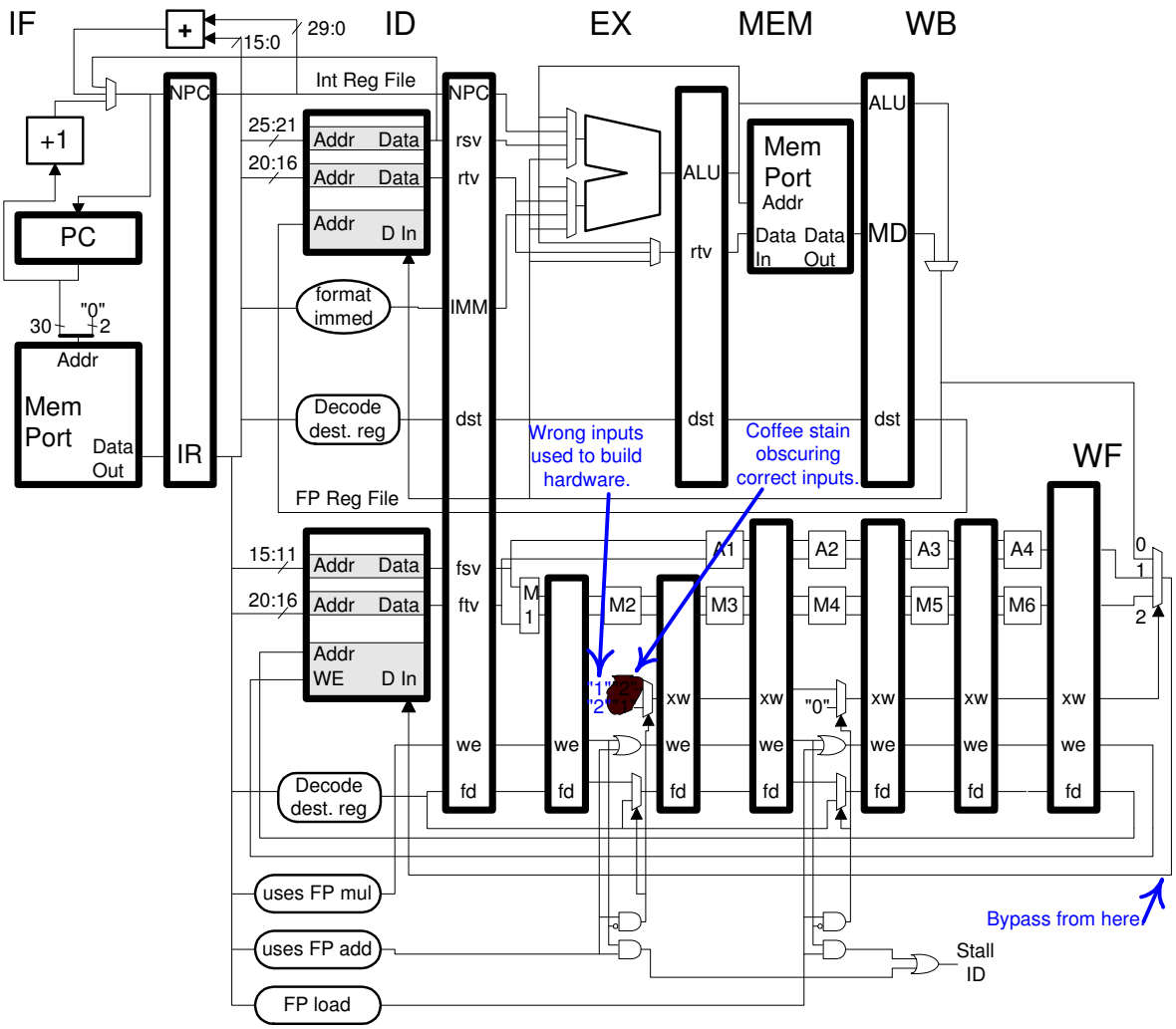
(*b*) Determine the CPI for a large number of iterations.

(*c*) Add exactly the bypass connections that are needed.

```
LOOP:
 mul.d f2, f2, f4
 bneq r1,0 LOOP
 addi r1, r1, -1
```

Problem 2: Due to a coffee spill the implementation below has a flaw: The inputs to the M2-stage XW mux have been reversed, the top input should be a 2 but is a 1, and the lower input should be a 1 but is a 2. There are no other flaws, in particular the control signal for the mux has been designed for a 2 at the upper input and a 1 at the lower input.

You are stranded alone on an island with this flawed implementation and to get off the island you need the result computed by the code below. The code was written for a normal MIPS implementation and will not compute the correct result on the flawed one. Re-write it so that it computes the correct result on the flawed implementation. (The solution must use the FP arithmetic units, do not simply implement IEEE 754 floating point using integer instructions.)




```
LOOP:
 add.d f2, f2, f4
 bneq r1,0 LOOP
 addi r1, r1, -1
```