

Name _____

Computer Architecture
EE 4720
Midterm Examination
Friday, 1 April 2005, 11:40–12:30 CST

Problem 1 _____ (25 pts)

Problem 2 _____ (30 pts)

Problem 3 _____ (25 pts)

Problem 4 _____ (20 pts)

Alias _____

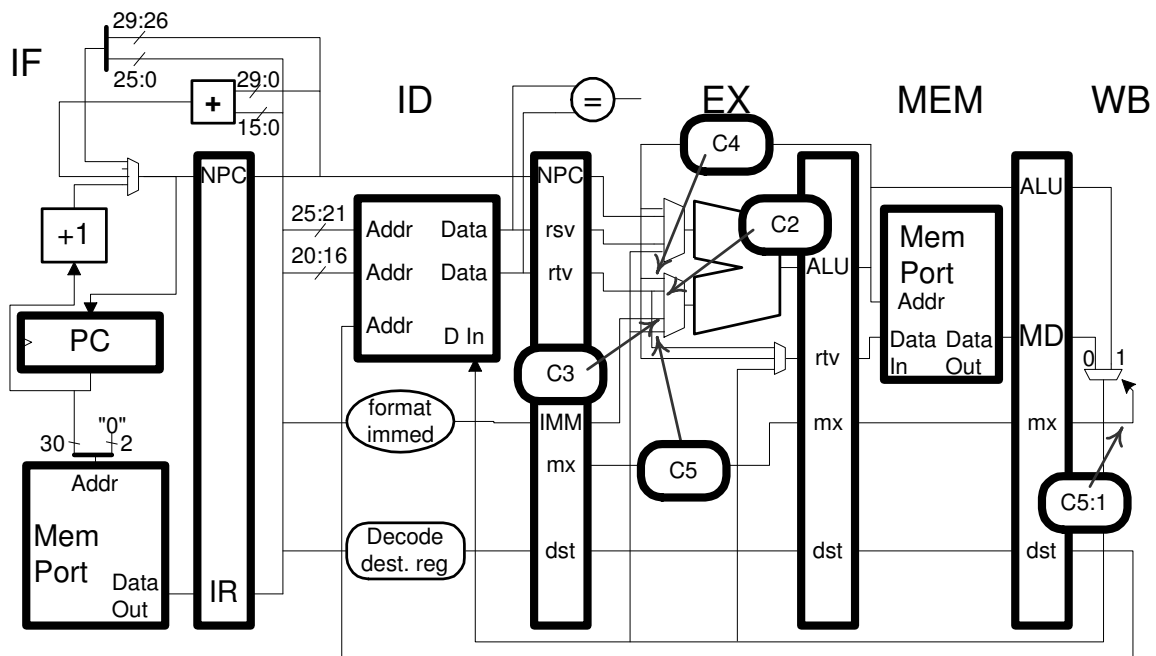
Exam Total _____ (100 pts)

Good Luck!

Problem 1: In the diagram below some wires are labeled with cycle numbers, indicating that the wire is used at that cycle. If a value on any labeled wire is changed the code would execute incorrectly.

- There are no branches or other control-transfer instructions.

- [15 pts] Write a program consistent with these labels.
- All register numbers must be made up; **use as many different register numbers as possible** while still being consistent with the labels.
- [10 pts] Why would there be no solution to the problem if the C5:1 label in WB were changed to C5:0?



Cycle: 0 1 2 3 4 5 6 7

	IF	ID	EX	ME	WB	
	IF	ID	EX	ME	WB	
	IF	ID	EX	ME	WB	
	IF	ID	EX	ME	WB	

Cycle: 0 1 2 3 4 5 6 7

Problem 2: In the diagram on the next page some wires are labeled with cycle numbers and corresponding values. For example, C1:8 indicates that at cycle 1 the pointed-to wire will hold an 8. Other wires are labeled just with cycle numbers, indicating that the wire is used at that cycle. If a value on any labeled wire is changed the code would execute incorrectly.

- Unlike other problems of this type all registers are different and there are no dependencies.
- The code contains at least one floating-point add and one floating-point multiply.

[10 pts] Write a program consistent with these labels; if a register number cannot be determined use rX or fX.

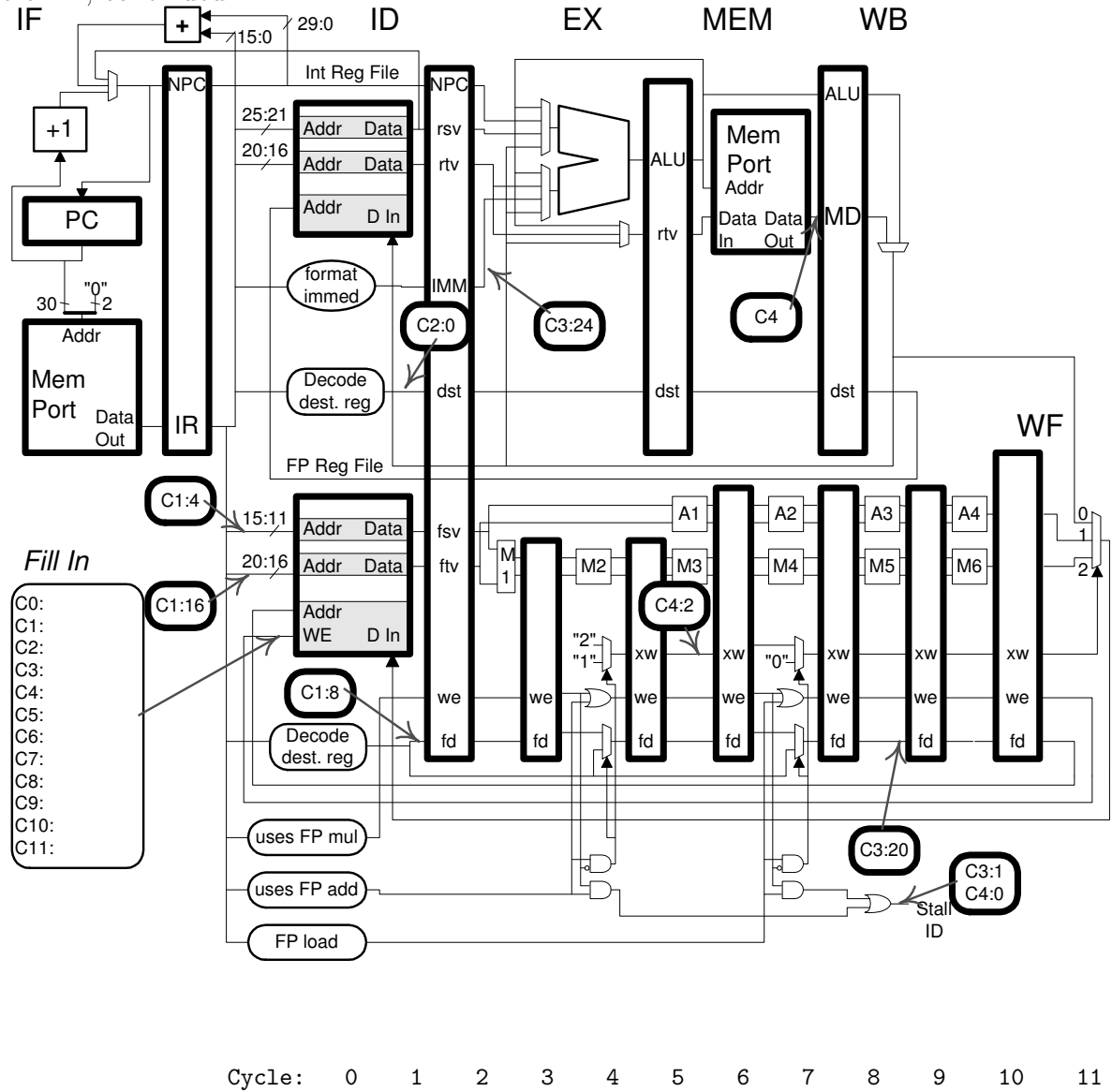
[5 pts] Complete the pipeline execution diagram.

[5 pts] Fill in the box on the lower-left of the diagram.

[5 pts] Your answer should have a FP multiply instruction. Explain how you knew it was a multiply. (Don't answer "because I already found the add.")

[5 pts] Your answer should have a FP add instruction. Explain how you knew it was an add. (Don't answer, "because I already found the multiply.")

Problem 2, continued:



IF ID

IF ID

IF ID

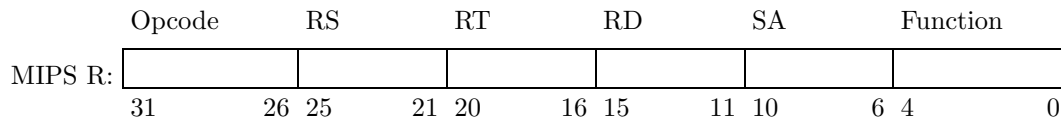
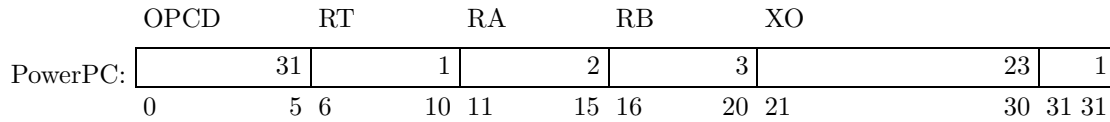
Cycle: 0 1 2 3 4 5 6 7 8 9 10 11

Be sure to complete all parts, including the justification for add and multiply.

Problem 3: Answer each question below.

(a) The encoding of the PowerPC `lwzx r1, r2, r3` instruction is illustrated below, followed by the Type-R MIPS instruction format. [6 pts]

- If a field in the illustrated PowerPC instruction format has a counterpart in the MIPS R format draw an arrow between the fields. For example, an arrow should be drawn from OPCD to Opcode. Pay close attention to the register fields.
- If fields connected by an arrow are different sizes explain the significance of the difference. (What advantage or disadvantage would the format with the larger field have, if any.)



(b) Suppose that your favorite program is both in the SPEC CPU2000 suite and in the suite used by a popular personal computing magazine and that the input data used for testing the program are also identical. You are considering buying two computers, *A*, and *B*. The spec testing shows that your favorite program is faster on *A* but the magazine's test shows that it is faster on *B*. The exact same model of machine *A* is used for running the spec test and the magazine's test, likewise for *B*. [6 pts]

- Provide a possible reason for the discrepancy, the reason should help explain why SPEC is used by the CPU research and development community. *Note: In the original exam the text after discrepancy was offered as a hint.*

(c) SPEC members and associates are drawn from computer manufacturers, other industries, academia, and elsewhere. [6 pts]

- Would you trust SPEC benchmark results more (or less) if computer manufacturers were not allowed to join SPEC? Explain.

(d) In class we saw that the optimized π program (reproduced below) ran faster than the unoptimized version (good) but also had higher CPI than the unoptimized version (bad). *Note: the words “than the unoptimized version” was not included in the original exam.* [7 pts]

Why was the CPI higher?

Hint: It has to do with something you learned early in grade school.

```
double i, sum = 0;
for(i=1; i<5000; )
{
    sum = sum + 4.0 / i;
    i += 2;
    sum = sum - 4.0 / i;
    i += 2;
}
```

Problem 4: Answer each question below.

(a) MMX and VIS are examples of ISA extensions that add packed-operand data types and instructions. [7 pts]

How do packed-operand data types and instructions improve performance?

Show a code example that can use such instructions and explain how they would be used.

(b) Name an advantage and a disadvantage that RISC's fixed-size instructions have over CISC's variable length instructions.[6 pts]

Advantage:

Disadvantage:

(c) A trap instruction is something like a subroutine call to the operating system. [7 pts]

So why couldn't it just specify the address of the trap handler?

What does the trap instruction specify (in SPARC but not MIPS) in place of an address and how does execution actually reach the trap handler.