Name _____

Computer Architecture

EE 4720

Midterm Examination

Monday, 29 March 2004,   13:40–14:30 CST

Problem 1 _____ (40 pts)

Problem 2 _____ (25 pts)

Problem 3 _____ (35 pts)

Alias _____   Exam Total _____ (100 pts)

Good Luck!

Problem 1: In the diagram below some wires are labeled with cycle numbers and values that will then be present. For example, $\boxed{\text{C3:0}}$ indicates that at cycle 3 the pointed-to wire will hold a 0. Other wires are labeled just with cycle numbers, indicating that the wire is used at that cycle. If a value on any labeled wire is changed the code would execute incorrectly. There are no stalls during the execution of the code. The first instruction (or) is shown (but don't forget to add the registers). [40 pts]
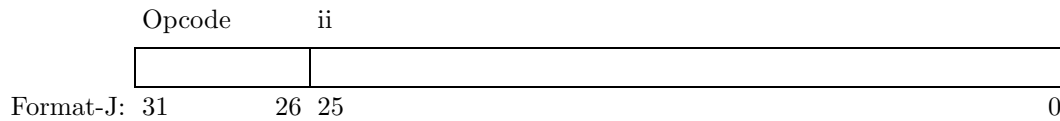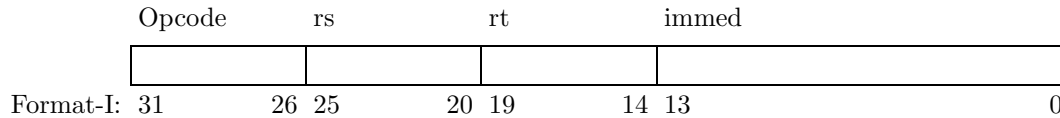
☐ Write a program consistent with these labels.

☐ Show the address of every instruction.

☐ Show every register number that can be determined and use r10, r11, etc. for other register numbers.

☐ Show the exact instruction (they can all be determined). For example, not just a load, but a load ____.
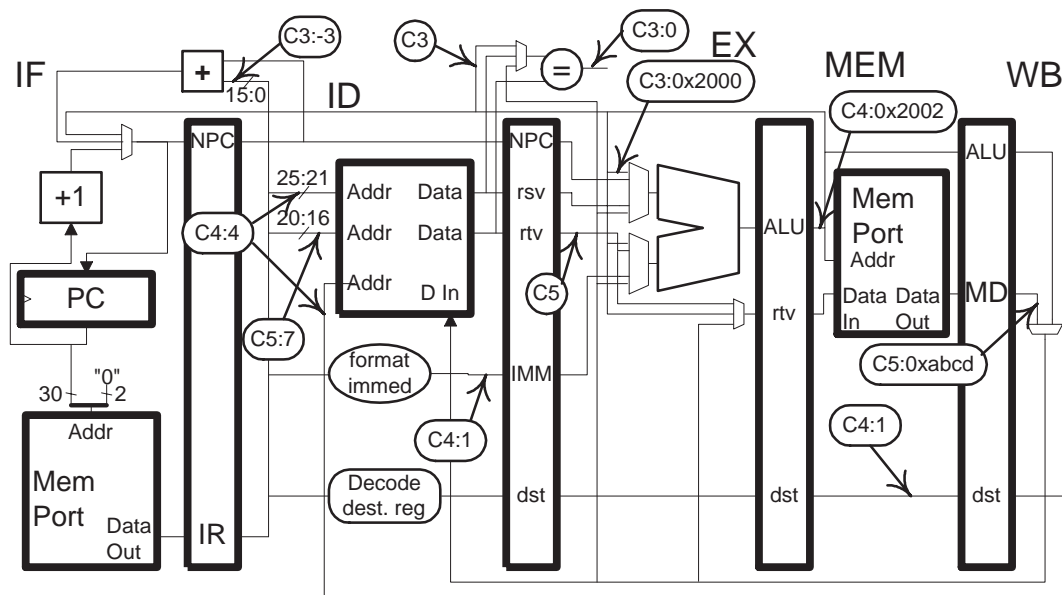
Insn Addr	Cycle:	0	1	2	3	4	5	6	7	8
0x1000: or		IF	ID	EX	ME	WB				
			IF	ID	EX	ME	WB			
				IF	ID	EX	ME	WB		
					IF	ID	EX	ME	WB	
						IF	ID	EX	ME	WB
	Cycle:	0	1	2	3	4	5	6	7	8

2

Problem 2: Consider a new ISA, F-MIPS, similar to MIPS-I except that it has 64 rather than 32 general purpose registers. F-MIPS has R, I, and J instruction formats like MIPS-I but with modifications to handle the larger number of registers. A goal of F-MIPS is to have all of MIPS-I instructions.

Possible instruction formats are shown below. Some details of Format R are omitted and are the subject of the first question.

```
            Opcode       rs         rt         rd        sa        func
           ┌──────────┬──────────┬──────────┬──────────┬─────────┬────────┐
           │          │          │          │          │         │        │
           └──────────┴──────────┴──────────┴──────────┴─────────┴────────┘
Format-R:  31        26 25       20 19      14 13       8 7      ? ?       0
```

```
            Opcode       rs         rt              immed
           ┌──────────┬──────────┬──────────┬─────────────────────────────┐
           │          │          │          │                             │
           └──────────┴──────────┴──────────┴─────────────────────────────┘
Format-I:  31        26 25       20 19      14 13                          0
```

```
            Opcode       ii
           ┌──────────┬──────────────────────────────────────────────────┐
           │          │                                                   │
           └──────────┴──────────────────────────────────────────────────┘
Format-J:  31        26 25                                                0
```
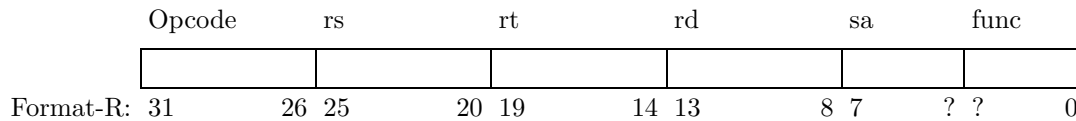
☐ [6 pts] Describe a problem with Format-R F-MIPS instructions using the Format R shown above.

☐ [7 pts] Fix the problem in Format R (show the changes in the illustration above). Explain the impact (this is important) on the coding of F-MIPS instructions.

☐ [6 pts] Explain an impact on typical F-MIPS Format-I instructions (compared to their MIPS-I counterparts) that would not apply to Format-R instructions.

☐ [6 pts] Why is something going to have to be done about `lui`? Describe a new version of `lui`, possibly using a new format, that would fix the problem. *Hint: That's load upper immediate.*

Problem 3: Answer each question below.

(*a*) A company has to choose between developing two new implementations of their ISA. Implementation *A* would have a peak (result) score of 2200 and a base (baseline) score of 2000 on the SPEC CINT2000 benchmarks. Implementation *B* would have a peak (result) score of 2150 and a base score of 2100 on the benchmarks.

[0 pts] Which implementation should the company choose? *Hint: Either answer is correct.*

[9 pts] Why? Your reason should say something about the difference between the peak and base scores and about the company's customers.

(*b*) Should a BCD data type be added to a modern general-purpose ISA?

[8 pts] Explain why or why not, using the criteria discussed in class for adding data types to an ISA. (Discuss specific features of BCD, don't give an answer that could apply to any data type.)

(c) Re-write the SPARC code fragment below in MIPS-I. Use as few instructions as possible. [9 pts]

```
 ! Notes: r0 is the zero register;  destination is rightmost register;
 !        be means branch if equal.  Use the same register names.

subcc %r1, %r2, %r0
add   %r3, %r4, %r5
be    TARG
xor   %r6, 10, %r6
```

(d) The code below includes a hypothetical MIPS predicated instruction. Re-write the code using real MIPS instructions. [9 pts]

```
      sub r3, r6, r7
 (r1) add r2, r3, r4
      xor r5, r8, r7
```