

Problem 1: One question when extending an ISA from 32 to 64 bits is what to do about the shift instructions. Because of the way that the shift instructions are encoded in MIPS two new shifts (of each type) were added to MIPS-64.

(a) What do you think the MIPS-32 `sra` instruction should do in MIPS-64? Remember that an implementation of MIPS-64 must run MIPS-32 code correctly. Please answer this question before answering the next parts (but feel free to look at the questions). *Hint: Any serious answer will get full credit. A smart-alec answer will get full credit only if it's particularly witty.*

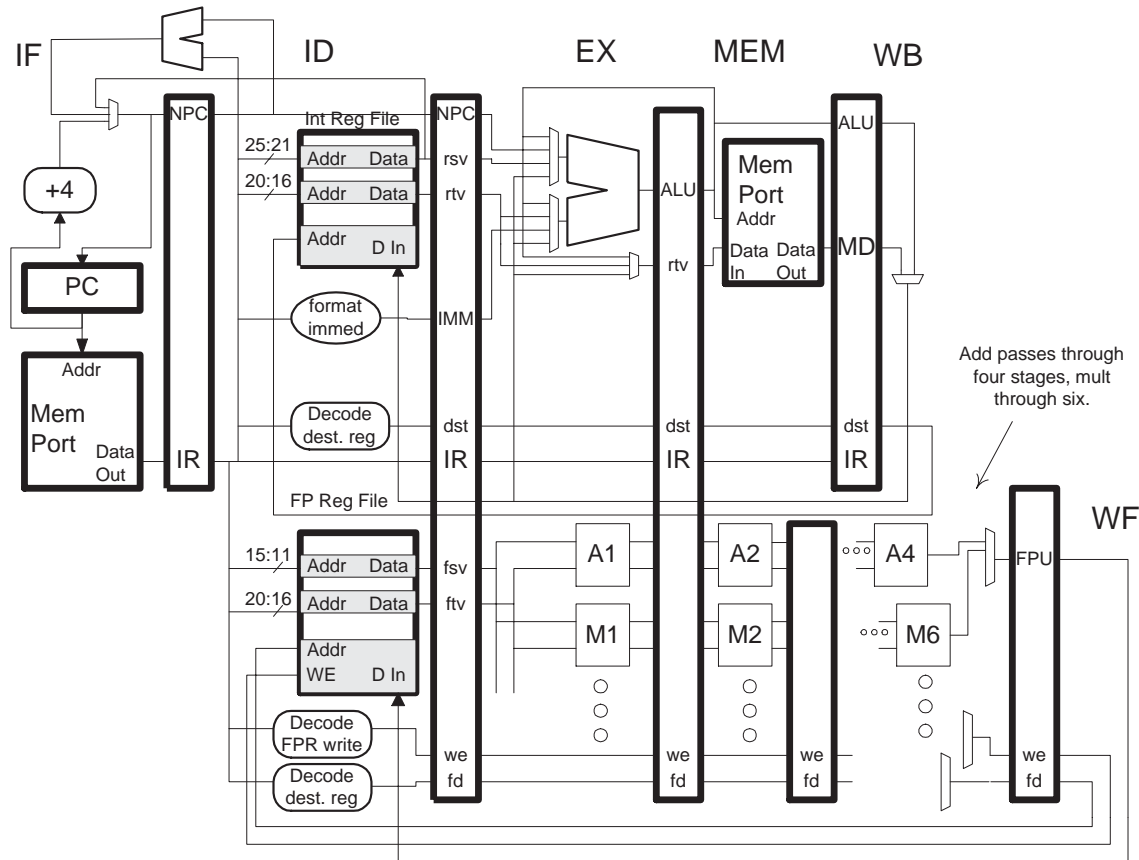
(b) Give two reasons why the MIPS-32 `sra` (not `srav`) instruction could not be used for all right arithmetic shifts needed in a 64-bit program.

(c) What are the new MIPS-64 shift right arithmetic instructions? Give the mnemonics.

(d) Why were two (as opposed to one) new shift instructions of each type added to MIPS-64?

Problem 2: Do the Problem 2 (a) through (d) from the Fall 2003 EE 4720 final exam (the one on floating point instructions). (<http://www.ece.lsu.edu/ee4720/2003f/fe.pdf>) Do not look at the solution until after you have solved the problem or gave it a good try.

Problem 3: In the diagram below the *we* pipeline latches carry write enable signals for use in floating point writeback. If the functional units were arranged differently the *we* pipeline latches could be used as a reservation register (for detecting WF structural hazards).



- Redraw the diagram with that arrangement. *Hint: Try to use the *we* signal in the diagram above for a reservation register. Figure out why that won't work and come up with a solution.*
- Suppose the ID stage has boxes `uses FP ADD` and `uses FP MUL` to detect which (if any) floating point functional unit an instruction would use. Design the control logic to generate a stall signal if there would be a write float structural hazard.
- Add the connections necessary for a `lwc1` instruction. Include the connections needed to detect a WF structural hazard (as was done for `ADD` and `MUL` in the previous part).