Name _____

Computer Architecture
EE 4720
Midterm Examination

Friday, 21 March 2003, 13:40–14:30 CST

Problem 1	_____	(30 pts)
Problem 2	_____	(30 pts)
Problem 3	_____	(40 pts)
Exam Total	_____	(100 pts)

Alias _____

Good Luck!

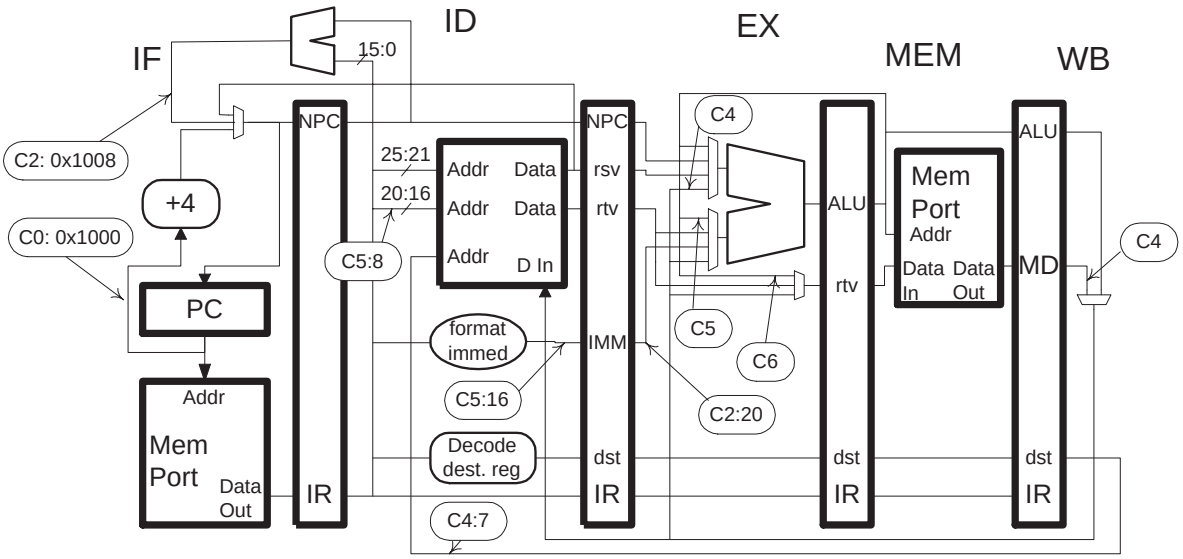
Problem 1: In the diagram below certain wires are labeled with cycle numbers and values that will then be present. For example, C5:8 indicates that at cycle 5 the pointed-to wire will hold an 8. Other wires are labeled just with cycle numbers, indicating that the wire is used at that cycle. There are no stalls during the execution of the code.[30 pts]

☐ Write a program consistent with these labels.

☐ The branch is taken. Use labels for branch targets and label the target line.

☐ Show the address of every instruction.

☐ Fill in every register number that can be determined and use `r10`, `r11`, etc. for other register numbers.




```
Cycle                  0  1  2  3  4  5  6  7  8

                       IF ID EX ME WB

                          IF ID EX ME WB

                             IF ID EX ME WB

                                IF ID EX ME WB

                                   IF ID EX ME WB

Cycle                  0  1  2  3  4  5  6  7  8
```

Problem 2: The CISC-A ISA is making its world premier in this exam!

- It has 32 integer registers (the MIPS names can be used) and the address size is 32 bits.
- Each operand in each instruction can use any appropriate addressing mode, including register, immediate, and the full range of memory addressing modes described in class.
- Instructions are variable size, the entire first byte is the opcode.

(*a*) Re-write the code below in CISC-A, making up appropriate instructions as needed. [10 pts]

☐ Take advantage of CISC-A's characteristics to reduce code size within the loop (primary goal) and outside the loop (secondary goal). (See the next problem.)

☐ Take advantage of: the available *addressing modes* (memory, register, and immediate), the *variable instruction size*, and *operand flexibility*.

☐ A correct solution includes at least three big-improvement-over-MIPS instructions.

☐ Identify non-MIPS addressing modes used.

```
 lui $t0, 0x1234
 ori $t0, $t0, 0x5678
 lw $t2, 0($s0)
 lw $t2, 0($t2)
 addi $t3, $t0, 0x1000
LOOP:
 lw $t1, 0($t0)
 addi $t0, $t0, 4
 bne $t0, $t3  LOOP
 add $t2, $t2, $t1
```

(*b*) Describe a possible coding for three of the CISC-A instruction used above. Don't choose three similar instructions. [10 pts]

☐ It should be obvious (to a computer engineer) that the full range of operands is available.

☐ The coding must follow the • bulleted • points above.

☐ Instruction size should be small, though not the absolute minimum size.

Problem 2, continued: Consider a second ISA, CISC-B, which differs from CISC-A in the following RISCy ways:

- Only load and store instructions can access memory.
- Each instruction has a fixed set of operand types, for example, an `addi` might be limited to one register destination, one register source and one immediate source.
- CISC-B still has variable-size instructions.

(*c*) Show how one such instruction might be coded. Try to choose a good example from the problem above. [5 pts]

☐ The coding should reflect and exploit CISC-B's operand restrictions.

(*d*) Show two program fragments: [5 pts]

☐ Show a program fragment that would be smaller in CISC-B than CISC-A. (No more than four instructions.)

☐ Show a program fragment that would be larger in CISC-B than CISC-A. (No more than four instructions.)

Problem 3: Answer each question below.

(*a*) Answer the following optimization questions. [10 pts]

☐ Explain the difference between front-end and back-end optimizations.

☐ Can typical front-end optimizations be performed by the back end? Explain using an example.

☐ Can typical back-end optimizations be performed by the front end? Explain using an example.

(*b*) It is important to computer manufacturers to have high SPEC benchmark ratings. For each technique of improving SPEC ratings, describe whether it will work, and if it won't describe why not. [10 pts]

☐ Try to have a favorable benchmark added to the suite by sending the name of the benchmark and a little something for their trouble (a bribe) to morally weak SPEC members. *In the exam as given the sentence started "Have a favorable . . .".*

☐ Modify the source code to the benchmarks, honestly improving performance on your system.

☐ Modify your compiler so that it honestly produces faster benchmark executables.

☐ Report results with certain benchmarks omitted.

(*c*) The typical ISA has one-, two-, four-, and eight-byte integers. [10 pts]

☐ Explain a possible benefit of having five-byte integers.

☐ Explain a difficulty with adding five-byte integers, taking in to account a certain feature (some would call it a restriction) of many RISC ISAs. *Hint: The name of the feature begins with an "a".*

(*d*) Provide the requested code examples and answer the questions. Two instructions suffice. [10 pts]

☐ Show code having a data dependency; circle the registers carrying the dependency.

☐ What is the name of the corresponding hazard?

☐ Show code having an anti dependency; circle the registers carrying the dependency.

☐ What is the name of the corresponding hazard?