

Name _____

Computer Architecture
EE 4720
Midterm Examination
Friday, 26 October 2001, 13:40–14:30 CDT

Problem 1 _____ (15 pts)

Problem 2 _____ (15 pts)

Problem 3 _____ (10 pts)

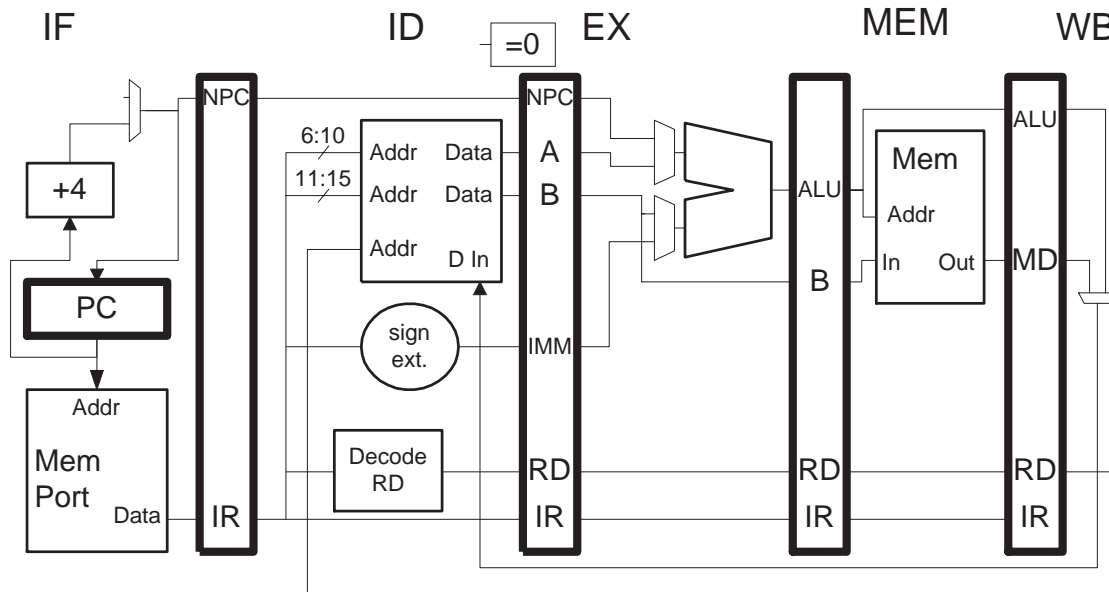
Problem 4 _____ (60 pts)

Alias _____

Exam Total _____ (100 pts)

Good Luck!

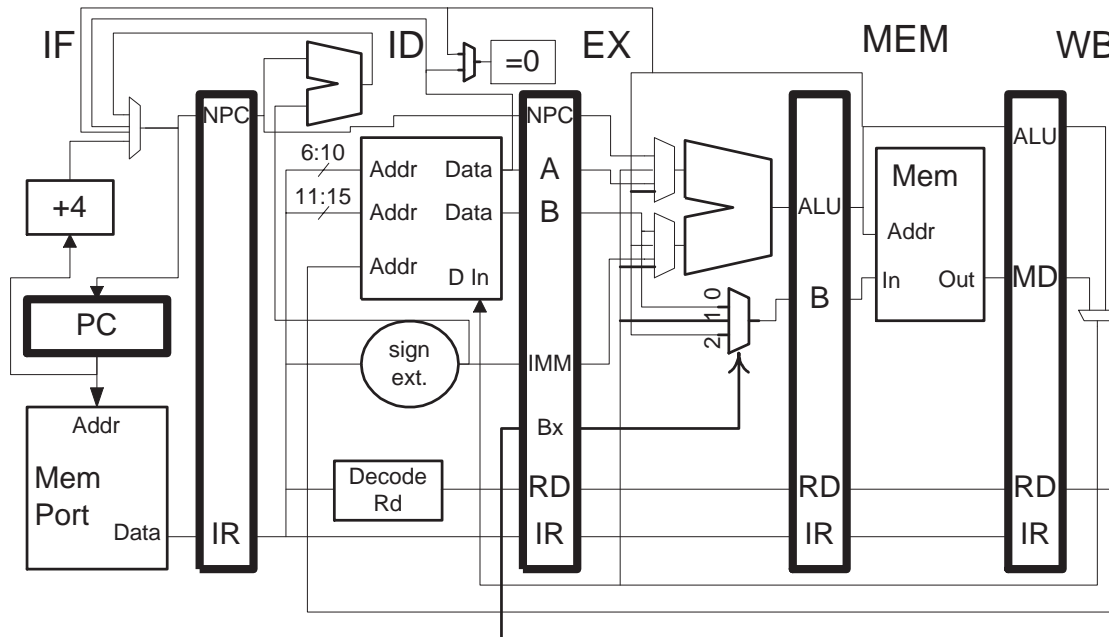
Problem 1: The DLX implementation below lacks bypass paths and, worse than that, lacks the hardware needed for control-transfer instructions.



- [5 pts] Add exactly the hardware needed so that the control-transfer instructions execute *as shown* below. Include a connection to the `=0` box used in determining whether a branch is taken.
- [5 pts] Add exactly those bypass paths necessary so that the code below executes *as shown*. Check the code carefully for dependencies, including all those related to the `jalr` instruction.
- [5 pts] Show the cycles in which each added wire will be used.

! Cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	
ori r1, r1, #15	IF	ID	EX	ME	WB									
bnez r1, SKIP		IF	ID	EX	ME	WB								
add r0, r0, r0			IF	IDx										
xor r0, r0, r0				IFx										
SKIP:														
sub r20, r20, r21						IF	ID	EX	ME	WB				
jalr r20							IF	ID	EX	ME	WB			
xor r0, r0, r0								IFx						
...														
add r15, r31, r0									IF	ID	EX	ME	WB	
or r16, r16, r15										IF	ID	EX	ME	WB
! Cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	

Problem 2: The DLX implementation below includes bypass paths into the EX/MEM.B register.



[5 pts] Write a program that uses all three paths into the EX/MEM.B register. *Hint: It's easy.*

[10 pts] Design the control logic for the multiplexor feeding the EX/MEM.B register. The control logic should be in the ID stage and feed into the ID/EX.Bx pipeline latch provided in the diagram above.

Problem 3: Registers `r1` and `r2` each contain a signed integer, call them i and j . Register `r10` contains an address, call the address A . Let $p = i \times j$.

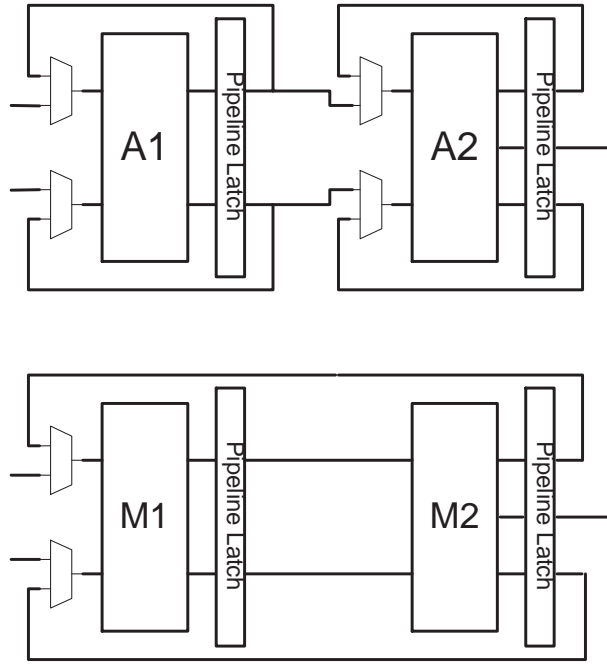
- [10 pts] Starting at address A write p in three formats: integer, double-precision floating-point, and single-precision floating-point. Maintain as much precision as possible.

Hint: A reasonable solution would use `movitof` and `cvtXtoY` instructions.

```
! Initially: r1 and r2 each contain an integer, i and j.
!           r10 contains an address.
!
!           At Mem[r10]    write i * j (integer format).
!           At Mem[r10+?] write i * j (double-precision FP)
!           At Mem[r10+??] write i * j (single-precision FP)
```

Problem 4: Answer each question below.

(a) In the two pipelined functional units below an instruction must pass through each segment twice. The A's are for FP addition and M's are for FP multiplication.



[10 pts] Complete the pipeline execution diagram below for a system using these functional units. Don't overlook the dependency through f6.

add f0, f2, f4

add f6, f8, f10

muld f12, f6, f14

muld f16, f18, f20

(b) The code below, which of course is not DLX, uses memory-indirect and autoincrement addressing.

```
lw r1, @(r2) ! Memory-indirect load.  
lw r4, (r5)+ ! Autoincrement  
lh r6, (r7)+ ! Autoincrement
```

[10 pts] Rewrite the code in DLX.

(c) The three types of interrupts discussed in class are traps, hardware interrupts, and exceptions.

[6 pts] For each one explain how the exception code is determined.

[6 pts] For each one explain where control returns after the handler completes.

(d) An ISA has two implementations, A and B ; each implementation has a well-written compiler.

[5 pts] Would the code compiled by A 's compiler run on implementation B ? Briefly explain.

[5 pts] A program is compiled using A 's compiler and B 's compiler. How might the compiled code differ? Provide a reason for the difference.

(e) You have become the owner of a large American computer company, congratulations.

[6 pts] How can you (legally) influence the decision-making process so that SPECs next benchmark suite does not unfairly put your company's products at a disadvantage? (Note: Bribery is illegal in the U.S.)

(f) DLX does not have delayed branches, but many other RISC ISAs do.

[6 pts] What is a delayed branch and how does it help?

(g)

[6 pts] How and why is the CPI affected in an implementation re-designed for a higher clock frequency?