EE 4720 Homework 5 Due: 24 April 2000

Problem 1: The code below is run on three machines each using a slightly different one-level branch predictor. Each machine's branch predictor uses a 1024-entry BHT. The first machine uses 2-bit saturating counters (as described in class), the second machine uses the 2-bit prediction scheme illustrated in Figure 4.13 of the text, and the third uses a 3-bit saturating counter. (The scheme illustrated in Figure 4.13 uses two bits, but it's not a saturating counter.) Find the prediction accuracy for each scheme on each branch instruction for a large number of iterations.

! r1 is initially set to a large value. LOOP1: subi r1, r1, #1 beqz r1, EXIT andi r2, r1, #6 bneq r2, SKIP1 add r3, r3, #1 SKIP1: andi r2, r1, #2 bneq r2, SKIP2 add r3, r3, #1 SKIP2: j LOOP1 EXIT:

Problem 2: What is the largest BHT size (number of entries) for which there will be collisions between at least two branches in the code above?

Problem 3: The program below runs on a system using a gselect branch predictor with a 14-bit branch history and a 2^{22} -entry BHT.

Show the value of the global branch history just before executing each branch after a large number of iterations. (The branch can be taken or not taken.) Also show the address used to index (lookup the value in) the BHT.

Determine the prediction accuracy of each branch assuming no collisions in the BHT.

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! r2 is initially set to a large value.
LOOP1: ! LOOP1 = 0x1000
addi r1, r1, #2
LOOP2: ! LOOP2 = 0x1080
 subi r1, r1, #1
bneq r1, LOOP2
A: ... ! Nonbranch instructions.
 addi r1, r1, #3
LOOP3:
       LOOP3 = 0x1100
 subi r1, r1, #1
bneq r1, LOOP3
B: ... ! Nonbranch instructions.
 subi r2, r2, #1
LINE: ! LINE = 0x1180
bneq r2, LOOP1
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Problem 4: Suppose the problem above ran on a gshare branch predictor with a 10-bit branch history and a 2¹⁰-entry BHT. Determine addresses for LOOP1, LOOP2, LOOP3, and LINE for which there would be collisions in the BHT after a large number of iterations. (Try to retain program order.)