Problem 1:   Consider a version of the Chapter-4 DLX pipeline that uses the following implementation of Tomasulo's Approach: Each functional unit has two reservation stations, numbered as follows: 1 and 2 for EX, 3 and 4 for ADD, 5 and 6 for MUL, and 7 and 8 for DIV. The integer execution unit is one stage and has an initiation interval of 1; all floating point units units are four stages and also have an initiation interval of 1 (these are the Chapter-4 DLX pipeline functional-unit timings). There is no bypassing other than that provided by the common data bus, so the timings given in Table 4.2 don't apply. Assume that all integer instructions use the memory stage but none of the floating-point instructions do. Load and store instructions use the integer pipeline in the same way as other integer instructions (do not assume special load and store buffers, do not worry about cache misses, and especially don't worry about why cache misses are something one might worry about). Show a timing diagram for the code below executing on this system up to (and including) the second fetch of the first `ld` instruction. Assume that all register values are available when the fragment starts.

```
muld f10, f20, f22
addd f22, f10, f10
muld f24, f10, f26
subd f0, f10, f30
loop:
ld   f2, 0(r2)
subd f0, f0, f2
ld   f2, 8(r2)
subd f0, f0, f2
ld   f2, 16(r2)
subd f0, f0, f2
subi r3, r3, #1
addi r2, r2, #24
bnez r3, loop
```

Problem 2:   Design hardware implementing (m, n)-bit correlating branch prediction for the Chapter 3 DLX pipeline using a 2^h-entry BHT. (Ignore the fact that a branch prediction in the Chapter 3 DLX pipeline is not useful.) The hardware should generate a PRED_TAKEN signal in ID when the instruction is a branch and is predicted taken. Don't forget to update the BHT based on branch outcome. Draw a logic diagram showing details of added hardware. Include address, data, and read/write signals for the BHT and any other storage devices used. Show the execution of a branch on the modified pipeline, indicating where important actions take place (*e.g.*, BHT written, prediction ready).